Design-oriented measurements of high-efficiency PAs for high PAR signals using an NI-based platform

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Outline

• Overview of approaches for improving efficiency at power back-off
  • Supply modulation (envelope tracking)
    • GaN PA design (10GHz carrier)
    • Supply modulator (100MHz switching)
    • Integration and modeling
  • Outphasing
    • Quasi-MMIC isolated and non-isolated
    • Measurements of load modulation internal to the PA
• Measurement challenges and approach to nonlinear measurements based on NI equipment in a LabView meta-instrument environment
Main challenges in PA design

- Challenge 1: efficiency drops as output power drops
- Challenge 2: efficient PAs are nonlinear
- Challenge 3: load can vary
Transmitter architectures

- Need second PA
- Is the added complexity worth it?

**Doherty PA:**
- 6dB back-off
- 2 RFPAs, different size and bias
- BW limitation

**Outphasing (LINC):**
- 2 saturated RFPAs
- Isolated and non-isolated

**Envelope tracking:**
- RFPA and dynamic power supply
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Supply-Modulated Transmitters

High-efficiency PA (e.g. harmonically-tuned)
- Improve maximum PA efficiency at a chosen power level with sufficient bandwidth for broadband signals

Efficient Supply Modulator
- Maintain PA efficiency at average power by varying the drain supply voltage
- Enable high slew rates for tracking broadband signals
- Introduce minimal reduction in overall efficiency

Linearization
- Restore linearity by identifying sources of distortion to simplify DPD

Integration and packaging
- Integrate supply modulator with PA with minimal loading
- Thermal management
- Integration of various drivers
High-efficiency PA design

- Transistor power dissipation dominates
  - Reduced conduction angle
  - Avoids $v_{ds}$-$i_{ds}$ overlap, power dissipation

- Waveform shaping (e.g. class F)
  - Voltage squaring, current peaking
  - 2$^{nd}$ harmonic short allows $2f_o$ current
  - 3$^{rd}$ harmonic open allows $3f_o$ voltage

\[ PAE = \frac{P_{\text{out}} - P_{\text{in}}}{P_{dd}} \]
\[ \eta_d = \frac{P_{\text{out}}}{P_{dd}} \]
Effects of 2nd and 3rd harmonic

Consistent small-signal gain contours indicate that correct S-parameters were correctly de-embedded from load pull data after each cut.

<table>
<thead>
<tr>
<th></th>
<th>2nd Harmonic</th>
<th>2nd/3rd Harmonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power</td>
<td>31.6W</td>
<td>31.6W</td>
</tr>
<tr>
<td>Drain Efficiency</td>
<td>77%</td>
<td>85%</td>
</tr>
<tr>
<td>Power Consumed</td>
<td>41.0W</td>
<td>37.2W</td>
</tr>
<tr>
<td>Power Dissipated</td>
<td>9.4W</td>
<td>5.6W</td>
</tr>
</tbody>
</table>

2nd harmonic and 2nd/3rd harmonic load pull for the TGF2023-10 GaN HEMT in chip/wire configuration biased at 28V drain voltage and with 300mA quiescent current.
High-Efficiency PA Design for SM

- PA design has to take into account:
  - small signal gain
  - efficiency and
  - output power over a range of supply voltages corresponding to an input envelope range

- Use TriQuint 0.15um GaN:
  - 20V CW
  - 100um SiC substrate
  - 60um diameter vias
  - 240, 300 and 1200 pF/mm^2
  - 50Ω/sq TaN resistors

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Typical</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMAX</td>
<td>Vds = 20 V</td>
<td>1.15 A/mm</td>
</tr>
<tr>
<td>Peak Gm</td>
<td>Vds = 20 V</td>
<td>380 mS/mm</td>
</tr>
<tr>
<td>Vp</td>
<td>Ids = 1 mA/mm</td>
<td>-3.5 V</td>
</tr>
<tr>
<td>BVGD</td>
<td>Ig &lt; 1mA/mm</td>
<td>50 V</td>
</tr>
<tr>
<td>Ft</td>
<td>20V-200mA/mm</td>
<td>38 GHz</td>
</tr>
<tr>
<td>FMAX</td>
<td>20V-200mA/mm</td>
<td>140 GHz</td>
</tr>
</tbody>
</table>

- Modeling:
  - Fit class Ab/B over a range of Vds
  - Pulsed IV at 25 and 85 deg C
  - S-parameters at 5, 10, 15, 20 V for Idq=10 and 100mA/mm
  - Load pull PAE and power tuned at Vd=20V
Example GaN15 reticle

- Class-E PA
  - 10W

- Class-AB PA

- Class-AB
  - 10GHz, 4W
  - Driver 20GHz
  - HI-PA

- 10GHz + 20GHz PA
  - HI-integrated

- PA + Cascode Modulator

- iDSM2 Bootstrap
  - 10W, G_{sat}=20dB

- iDSM2 Pull-up

- Test structures
  - iDSM2 Active pull-up

- Outphasing
  - iDSM2 Active pull-up + level-shifter
High-Efficiency X-band MMIC PAs

Fixture

Carrier plate assembly

EM models for bondwires included in MMIC design

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Examples of single PA X-band MMICs

Circuit B:
2-Stage MMIC, combines four 10x90um, 3.8mmx2.3mm

Circuit F
Single stage, two 10x100um, 2.0mmx2.3mm

Circuits D/ E
Single stage, 10x100um, 3.8mmx2.3mm and 12x100um, 2.0mmx2.3mm

Output power from 9.5 to 12GHz

PAE from 9.5 to 12GHz
Static Supply Modulation Performance

### Circuit B - Drain Voltage Sweep

- $V_d = 20.0V$
- $V_d = 17.5V$
- $V_d = 15.0V$
- $V_d = 12.5V$
- $V_d = 10.0V$
- $V_d = 7.5V$
- $V_d = 5.0V$

### Circuit E - Drain Voltage Sweep

- $V_d = 20.0V$
- $V_d = 18.0V$
- $V_d = 16.0V$
- $V_d = 14.0V$
- $V_d = 12.0V$
- $V_d = 10.0V$
- $V_d = 8.0V$
- $V_d = 6.0V$

<table>
<thead>
<tr>
<th>Circuit</th>
<th>B</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max PAE (%)</td>
<td>59.9</td>
<td>66.8</td>
<td>55.7</td>
<td>69.4</td>
</tr>
<tr>
<td>Max $P_{out}$ (W)</td>
<td>13.2</td>
<td>3.98</td>
<td>3.22</td>
<td>2.64</td>
</tr>
<tr>
<td>Gate size (mm)</td>
<td>3.6</td>
<td>2.0</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td>W/mm</td>
<td>3.68</td>
<td>1.99</td>
<td>2.69</td>
<td>2.64</td>
</tr>
<tr>
<td>BW at PAE=45% (GHz)</td>
<td>1.6</td>
<td>0.77</td>
<td>1.88</td>
<td>1.95</td>
</tr>
<tr>
<td>$\Delta P_{out}$ (dB) / $\Delta V_{ds}$ (V)</td>
<td>11/12.5</td>
<td>3.3/7</td>
<td>4.8/9</td>
<td>5.3/8</td>
</tr>
</tbody>
</table>
X-band MMIC PAs – state-of-the-art

[1] [2] [3]
GaN Integrated Supply Modulators

- Switchers with integrated gate drivers
- η >90%, up to 200 MHz switching frequency, up to 15 W peak power

100 MHz, η>90%
10W peak
2.4 × 2.3mm in QFN package
Measured vs. simulated DSM

GaN half bridge switcher Meas/Simul

\[ \text{RMS error} = 100 \times \sqrt{\frac{\sum_{t=1}^{n}(V_{\text{out},t} - V_{\text{in},t})^2}{n}} \times \frac{1}{(V_{\text{out max}} - V_{\text{out min}})} = 4.5\% \]
PA performance with LTE signal

Instantaneous PAE, Gain and PDF of the output signal

Red = ET
Blue = 20V drain bias

PDF (P_Load_dBm)

PAE (%)

Gain (dB)

PDF ET

PDF Fixed bias

P_Load_dBm
Single-Chip Integrated ET-PA

- RF VHF/UHF input
- X-band input
- MMIC carrier board
- DC supply
- Switcher drive inputs
- DC supply, modulator
- Filter
- X-band modulated output
- DC supply, PA
Integration Issues: Linearization

Supply modulator issues:
- Supply sensitivity
- High slew rate
- Dynamic load
- Linearization

- SM modulator gain and phase distortion
- RFPA gain variation with $V_{\text{supply}}$
- Path delay difference between the $v_{\text{in}}$ and $V_{\text{supply}}$ paths occurs when both $v_{\text{in}}$ and $V_{\text{supply}}$ are changing over time
- Nonlinear memory
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Measured static drain impedance, fixed VDD

Vdd = 15V
Vg1=-2.8V, Vg2=-3.75V

Trends similar to simulations.

Real part is high at low frequencies and decreases to reach 1.5Ω at 500MHz.

At saturation, the real part remains under 20 Ω.

At low power, the drain impedance is highly capacitive and becomes almost purely real at compression.
Is it worth it? – S-band results

- Drive modulated conditions
  - Same W-CDMA signal
  - Same PA
  - Constant 32V $V_{dd}$
  - Achieves similar linearity

- Power consumption
  - ET requires 43% less power
  - ET operates 75% longer from battery

- Power dissipation
  - ET system produces 61% less heat
  - RF transistor operates 86% cooler

<table>
<thead>
<tr>
<th></th>
<th>Drive (A)</th>
<th>Optimized Traj</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak/Average Power</td>
<td>40W / 8.5W</td>
<td>40W / 8.5W</td>
</tr>
<tr>
<td>RFPA drain eff.</td>
<td>30%</td>
<td>76%</td>
</tr>
<tr>
<td>SM efficiency</td>
<td>N/A</td>
<td>69%</td>
</tr>
<tr>
<td>ACP at 5 / 10MHz</td>
<td>-57/-58.3 dBc</td>
<td>-55.7/-57.8 dBc</td>
</tr>
<tr>
<td>Transmitter efficiency</td>
<td>30%</td>
<td>52.5%</td>
</tr>
<tr>
<td>Supply power</td>
<td>28.3W</td>
<td>16.4W</td>
</tr>
</tbody>
</table>

PA Dissipation 19.8W, 100%
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PA element for outphasing PAs

- Single-stage
- Biased in class-B
- GaN MMIC PA (TriQuint 0.15 µm)
- 10 x 100 µm FET

- $V_{DD} = 20$ V, $V_G = -4.0$ V
- $f_0 = 10.1$ GHz
- Peak PAE = 70%
- $P_{out} = 2.7$ W
- Gain = 7.2 dB
Quasi-MMIC outphasing PA

Digital

Load pull contours for non-isolated combiner

Combiner:
- Isolated
- Non-isolated

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Internal PA Load Modulation

4-channel receiver

10 MHz Ref.

Driver

Coupler

MMIC PA

Low-Loss Coupler

RF Switches

Combiner

Power Meter

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Isolated Outphasing PA

- Finite isolation yields minimal load modulation
- PAs rotate in opposite direction around contours
- 0.4 – 1.7 dB internal PA $P_{\text{out}}$ imbalance caused by varying load
Non-Isolated Outphasing PA

- Load modulation shows slight CW rotation due to ±1.5 dB internal PA Pout imbalance
- Peak power occurs near peak PAE
- Minimum Pout of 3.6 dBm near edge of smith chart
Comparison

**Isolated**
- Peak $P_{out} = 35.8$ dBm / $36.8$ dBm
- Peak PAE = 41.6 % / 59%
- Integrated design: 1 dB less loss

**Non-isolated**
- Peak $P_{out} = 35.7$ dBm / $37$ dBm
- Peak PAE = 41.5 % / 60% (L=1.3dB)
- 8 % improvement in PAE at 4 dB OPBO
Effect of Power Unbalance

- 5±0.25 dB forced available power imbalance
- 2-9 dB internal PA Pout imbalance
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RF instrumentation in LabVIEW: an equation to be solved

THE GOOD
• Build a GUI with two clicks;
• Does not require any hard programming skills.

THE BAD
• LabVIEW code is difficult to read in big projects;
• Mix of GUIs, algorithms and instrumentation drivers;
• VISA interface is UNIVERSAL but...
• IVI is not:
  • Many DLLs;
  • No universal handle manager in LabVIEW;
  • Open/Closing sessions not convenient.

Nevertheless, there is a hope...
RF instrumentation is based on a very limited number of instruments:
- Power meters;
- RF Sources;
- DC power supplies;
- Scopes; and
- just one big analyzer.
A LabVIEW “open instrument”

“Redefining RF and Microwave Instrumentation with open software and modular hardware”

Existing approach on commercial PXI RF receiver

One single PXI module

Our approach for research and academics: open LSNA

Each element is modular

Versatile LabVIEW software

Goal: improve flexibility and creativity for researchers and academics in instrumentation.
LabVIEW for RF instrumentation

Available Instrumentation

Device Under Test

Arrays of Instruments

Meta-Instrument

- SCOPES
- SOURCES
- BIASES
- POWER METERS

Simulation Platform

- LSNA or user setup

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Arrays of instruments are defined by GUI and located in a global variable.

Some elements are already defined in the array of 'Sources'.

The array of 'Power meters' is currently empty.

Some GUIs (Sources and Scopes) includes PXI session init and close on the fly. Array can be deleted by clicking on the ‘X’.
Interactive control (useful with PXI sources). Open and Close PXI session on the fly if needed.

List of instrumentation previously defined in low-level drivers. (Typedef file)
Here is the list for VISA instruments.

All instrumentation in a lab previously defined in low-level drivers. Here we have 3 driver families: VISA, NI-FGEN (LF PXI) and NI-RFSG (RF PXI)
Make your own VI

Here is the library

Generic MDIF file can be read by Keysight ADS Data Display and specific file formats for AWR Microwave Office.
Example: Pout(Pin)

- Makes LabVIEW code lighter and clean;
- Generic Library highlights concepts more than drivers and acquisition protocol;
- Data-set fully integrated to simulation platform for direct measurement/simulation comparison.
Meta-instrument example:
2-port LSNA bench
Bench example, 2 ports
Calibration
Application: outphasing PAs

Measurements of internal load modulation

Requires Three identical 2-port RF LSNAs, but with different calibration matrices and initialization scripts (to setup the RF switches)
Measuring internal load modulation

1. Create an LSNA and copy it twice

2. Update the field Setup VI with the script to enable the correct RF-switch position.

3. Each of the 3 LSNA’s is calibrated independently.

4. All LSNA measurements are performed sequentially in just one call.
LF S-parameters under large signal condition is a minimal configuration to optimize filter between the LF modulator (PWM signal) and the RF-PA (Analog signal)
Create 2 different LSNAs.

One includes a downconverter, the other one doesn’t.

Each LSNA is related to its calibration matrix.

All LSNA measurements will be performed sequentially in a single ‘LSNA Measurements” call.

Measurements performed in LF 1 port LSNA + Power meters for the moment.
Problem to solve: Transistor models do not predict low-frequency (modulation) drain terminal impedance.
RF Envelope Input (volt) under 50 ohms

DC VD sweep compatible with LF VNA measurements

RF Average Power compatible with LF VNA measurements

S-par simulation performed with LSSP block (Harmonic Balance)

S-par simul will not take into account non-linear Gd
Example: Extracting a model...

Very simple circuit

\[ I = f(V_{in}, V_d) \]
\[ g_d = \frac{\partial I}{\partial V_d} \]

Table based model.
It included measured ID=f(Pav,Vd)
And extracted Gd

\[ |V_{in}(V)| = 10 \left\{ \frac{Pr_f(dBm)}{20} - 0.5 \right\} \]

: Non linear elements

EXTRACTED FROM I(V)

EXTRACTED FROM S-par

Very big capacitance
(transition between DC and LF)

gd compensation
Output capacitance
Resonance
(can be seen on real\{Y22\})
Example: comparison

**Measurements:**
Converted in Generic MDIF and loaded directly in the data display

**Simulations:**
Performed for the same sweep range

Comparison in the simulation platform
Example: results
Example: self-characterization

- Samplers characterized with NI PXI-5922 (15MS/s)
- Data displayed in Keysight ADS – Goal is to display in AWR MWO (but this needs improved Generic MDIF file format)
Summary

• LABVIEW-based LSNA under development
• Enables non-standard design-oriented measurements in a modular flexible fashion
• Measurement capability already demonstrated through several design applications:
  – Internal load modulation in outphasing PAs
  – Low-frequency drain impedance measurements under large-signal RF carrier excitation for a ET-PA