Nonlinear Electro-thermal modelling of packaged power GaN HEMTs

for the design of adaptive power amplifiers dedicated to

reconfigurable telecom payloads

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INTRODUCTION

The development of a new generation of transmitters at payload level operating with complex modulation scheme for telecom applications (i.e. multi-carrier operation) requires a high level of flexibility especially in terms of output power and efficiency of *SSPA* (Solid State Power Amplifier). This paper addresses the strategic emergent GaN power technology which is identified as the critical power technology for *RF* payload applications. Power flexibility is a critical identified need in transmitters at payload level since spacecrafts are built for a quite long period of 15 spaceflight years during which they are required to operate in non-constant traffic beams and variable coverage areas. This topic is extremely sensitive in power consumption of the global payload and researches focus on efficiency enhancement of *SSPA* assuming an output power dynamic range; as an example improving *SSPA* efficiency from 30 % to 35 % at constant output power would save *DC* power and decrease by 14 % the power consumption at payload level.
The emergent *GaN HEMTs* (high electron mobility transistor) devices are promising for power amplification particularly at high frequency level, high output power which has been demonstrated by several papers [1], [2].
This paper deals with the non linear modelling of commercialised *GaN* (Gallium Nitride) packaged transistor in L/S band which takes into account self-heating effects that appear mostly with high power *GaN* transistors, assuming that we do not have any information of the die size and package design.

PACKAGE MODEL EXTRACTION

The device used for this work is a packaged *10W GaN* high electron mobility transistor *(HEMT)* assembled in a metal-ceramic hermetic package. The device is composed of an active die mounted on a metallic thermal flange which is covered by a ceramic package. The extrinsic package elements have been extracted from S-parameters measurements in the [0.5-8GHz] frequency band under cold bias conditions (Vgs=0 V, Vds=0 V) of the device combined to a dedicated optimization process of the selected model topology.

SMALL SIGNAL MODEL

The extraction of the small signal model of the transistor stands for first modelling step. Typically, the small signal model is made up of specific linear elements which separately take into account the access elements of the package and the intrinsic elements of the active die. All model parameters have been extracted from pulsed scattering [S] parameters measurement in the [0.5-8GHz] frequency band under cold and hot bias conditions.

Model Topology

The small signal model topology used is composed of 15 linear components detailed on Fig.1 which can be divided into two distinct parts. On the one hand, a set of 8 parameters (*Lg, Rg, Cpg, Rd, Ld, Cpd, Rs and Ls*) represents the extrinsic elements which are linked to the die accesses and on the other hand, 7 parameters *(Gd, Rgd, Ri, Cgs, Cgd, Cds and Gm*) represent the intrinsic part of the active device. Capacitances (*Cpd, Cpg*) account for the parasitic effects due to pad connections, (*Lg, Ld and Ls*) represent the parasitic self inductances describing the effect of wire bonding while (*Rs, Rd and Rg*) stand for access losses, ohmic and Schottky contacts.

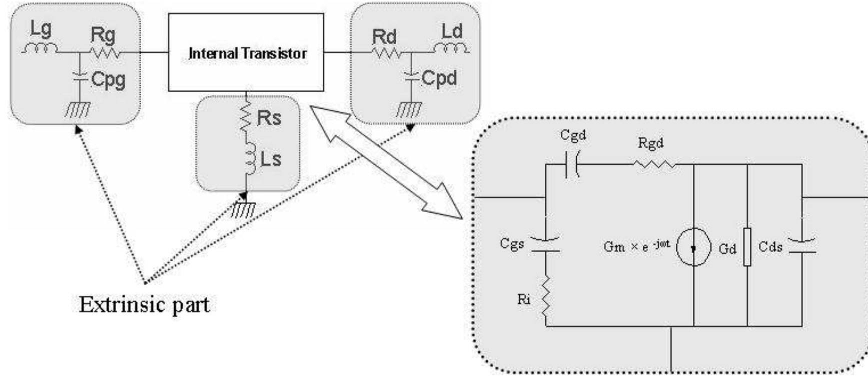


Figure 1 : Small signal model topology

Model extraction

The extraction method of the small signal model consists in finding the values of external parameters at any transistor bias point assuming that intrinsic die parameters are unknown; those will be deduced from established extrinsic values. From extrinsic measured scattering [S] parameters at a given bias point, the modeling algorithm extracts the intrinsic [Y] matrix according to a set of extrinsic values. Finally, given the intrinsic [Y] matrix, the intrinsic values are deduced from the specific equations shown below from (1) to (8) through the full transistor characterization. Extrinsic parameters have to be constant at any bias point while the intrinsic parameters are bias-dependent.

$$Cgd = \frac{-Im(Y12)}{\omega}\left[1+\left(\frac{Re(Y12)}{Im(Y12)}\right)^2\right] \tag{1}$$

$$Cgs = \frac{Im(Y11)+Im(Y12)}{\omega}\left[1+\left(\frac{Re(Y11)+Re(Y12)}{Im(Y11)+Im(Y12)}\right)^2\right] \tag{2}$$

$$Cds = \frac{Im(Y12)+Im(Y22)}{\omega} \tag{3}$$

$$Gd = Re(Y12)+Re(Y22) \tag{4}$$

$$Rgd = \frac{-Re(Y12)}{Cgd^2\omega^2}\left[1+\left(\frac{Re(Y12)}{Im(Y12)}\right)^2\right] \tag{5}$$

$$Ri = \frac{Re(Y11)+Re(Y12)}{Cgs^2\omega^2}\left[1+\left(\frac{Re(Y11)+Re(Y12)}{Im(Y11)+Im(Y12)}\right)^2\right] \tag{6}$$

$$A = Re(Y21)-Re(Y12),\ B = Im(Y21)-Im(Y12) \tag{7}$$

$$Gm = \sqrt{(A^2+B^2)(1+Ri^2Cgs^2\omega^2)},\ \tau = \frac{-1}{\omega}arctan\left[\frac{B+A\times Ri\times Cgs\times\omega}{A-B\times Ri\times Cgs\times\omega}\right] \tag{8}$$

The linear model extraction is based on S-parameters measurements from 500 MHz to 8 GHz at the selected bias point *(Ids_0 = 100 mA, Vds_0 = 50V).* This specific bias point has been selected for our future amplifier application as the typical bias point defined by the manufacturer able to provide a tradeoff between output power and drain efficiency.
After the modeling process, all parameter values of the small signal model are listed in the table below while the associated graphs in Fig.2 demonstrate the good agreement obtained between model and measurements aver the [0.5-8] GHz frequency band.

Lg (pH)	Cpg (fF)	Rg (Ω)	Rs (Ω)	Ls (pH)	Ld (pH)	Cpd (fF)	Rd (Ω)
7.96	255	0.78	0.03	78.7	54.2	25.7	0.25

Cgs (pF)	Cgd (pF)	Cds (pF)	Gm (mS)	Gd (mS)	Ri (Ω)	τ (ps)	Rgd (Ω)
7.8	0.106	0.92	377	2.6	0.6	7.1	12.65

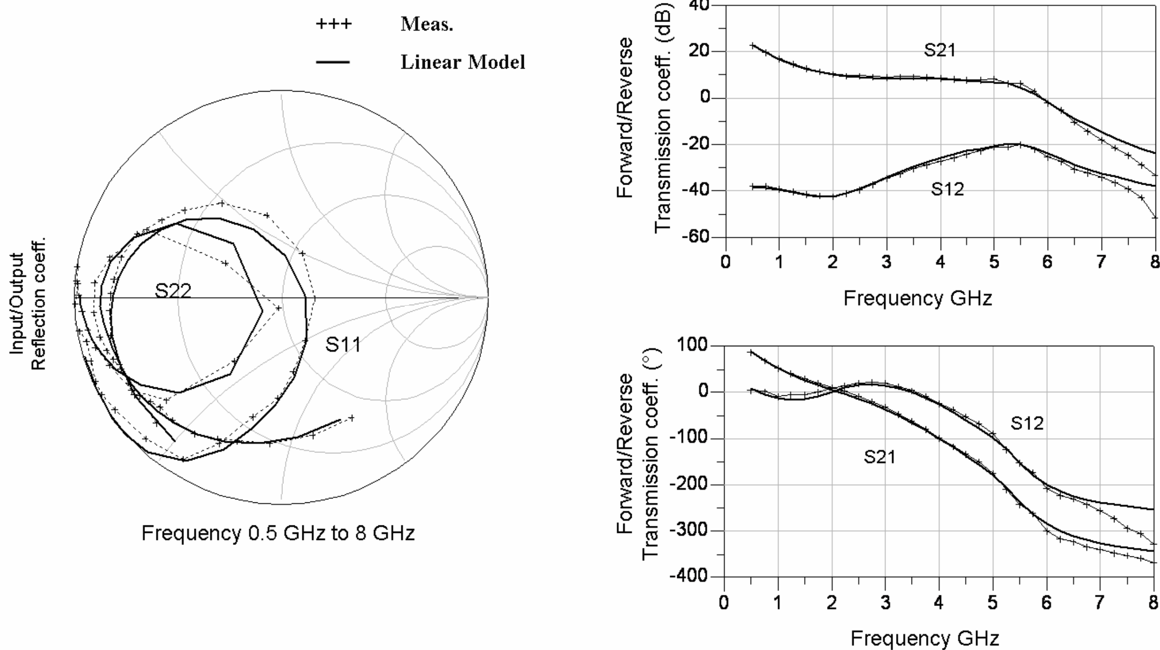


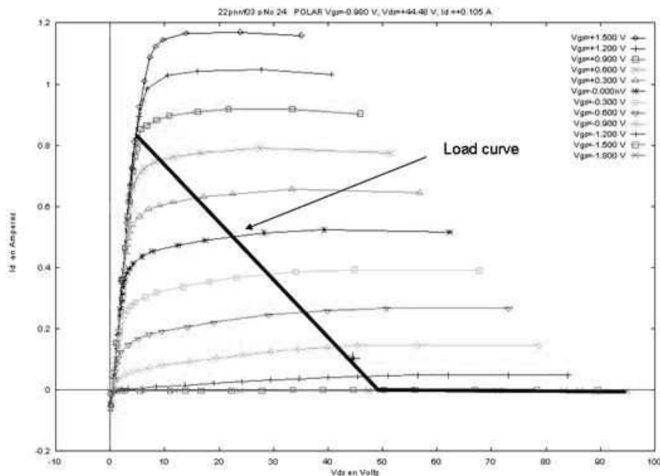
Figure 2 : Small Signal model vs pulsed [S] measurement at (Id=100 mA, Vd=50 V) quiescent bias point

NON LINEAR MODEL

In order to describe the device behavior at large input power levels, a nonlinear electrothermal model has been extracted from pulsed S-parameters and pulsed I-V measurements. The most critical non linear element is the current source which is modeled by Tajima's equation [3] that provides a good agreement of measured I-V curves from pinch off voltage to the full conduction locus while ensuring a good coherency with the equivalent transconductance and conductance at small signal level.

Cgs and Cgd Nonlinear capacitances

The description of the non linear behaviour of *Cgs* and *Cds* capacitances is based on a specific 1-D model [4]. This model describes each capacitance as a function of its own control voltage (*Vgs* or *Vgd*), since the non linear behaviour is extracted within the I-V locus along a selected load line closest to the one of the required operating case (i.e efficiency matching in our case). This load line (Fig.3) was selected to match the actual transistor load curve during the required power operation. Multi-polar extraction of internal parameters of the transistor gives us several *Cgs* and *Cgd* measured data depending on *Vgs* and *Vgd* voltages. Consequently, we get the non linear capacitance behaviour along the entire selected load line.



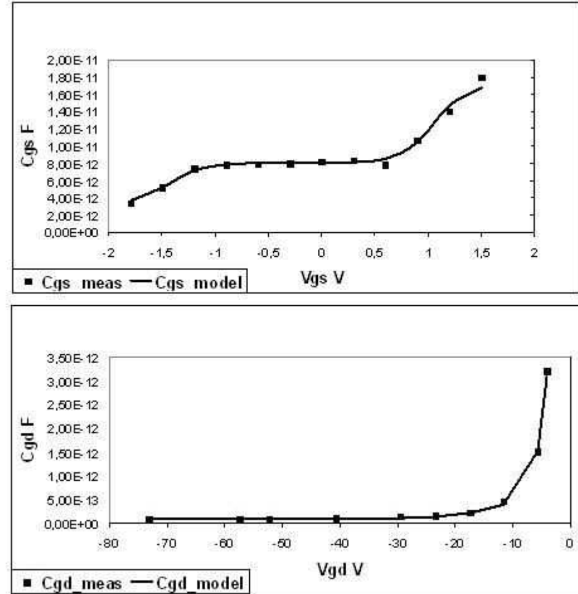


Figure 3 : 1-D nonlinear Cgs and Cgd values extracted on the selected load line and modeled with hyperbolic tangent functions. Square marks correspond to values extracted along the load line and solid lines correspond to the model.

Pulsed I–V Measurements and Current Source Extraction

Pulsed I-V measurements have been performed at the quiescent bias point (Ids=100mA, Vds=50V) using 400 ns width short pulse in order to get a quasi-isothermal measurement process. The intrinsic non linear topology is shown on Fig.5 where the current source describes the *HEMT* behaviour by using Tajima's equation. A dedicated measurement and modelling software developed at XLIM laboratory enables to directly extract the non linear model parameters knowing *Rg, Rd* and *Rs* resistors from [S] parameters characterization. Fig. 4 shows a comparison between pulsed I-V measurements and non linear modelling.

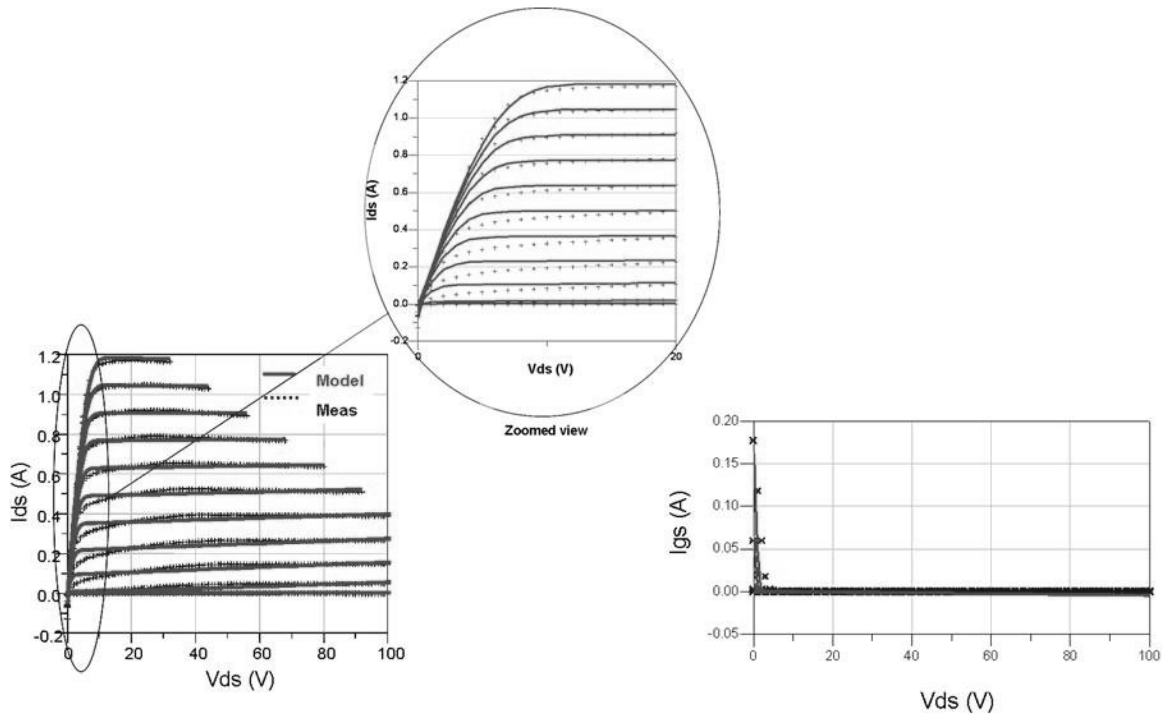


Figure 4 : 400 ns pulsed I-V measurements of the 10W GaN at quiescent bias point (Ids = 100mA, Vds = 50V). Solid lines correspond to the model whereas dot lines stand for measured data.

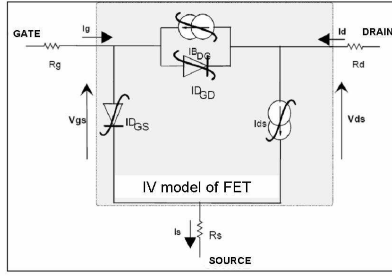


Figure 5 : Intrinsic nonlinear model topology for pulsed I-V measurement

The input diodes *IDgd* (gate-drain) and *IDgs* (gate-source) are modeled as nonlinear current sources using the following equations:

$$ID_{GD} = I_{sgd} \times (e^{ALPHA_GD \times V_{gd}} - 1) \quad (9)$$

$$ID_{GS} = I_{sgs} \times (e^{ALPHA_GS \times V_{gs}} - 1) \quad (10)$$

The thermal dependency of the current source is obtained by fitting I-V curves at different chuck temperatures which impose the temperature since pulsed I-V measurements are isothermal. Different parameters of the Tajima's current source are temperature dependent so that they are modeled by specific equations so that to be dynalically controlled by the actual operating temperature of the device within the circuit.

Thermal circuit

The thermal characterization of the power device is based on electrical measurement but there exists different means of measuring the temperature within a transistor. During the measurement process, we have to dissociate thermal effects against lag effects assuming that lag effects are mainly linked to the bias voltage point. Therefore, the thermal modeling process is performed by using pulsed I-V measurements at cold bias conditions *(0mA, 0V)* while the temperature is imposed by the thermal chuck.
The thermal resistance called *Rth* is the temperature difference across a structure when a unit of heat energy flows through it in unit time; it is expressed in *°C/W*.

$$R_{th} = \frac{\Delta T}{\Delta P_{diss}} \quad (11)$$

Usually, *Rth* is a nonlinear parameter versus the temperature; the drain current principle [5] permits to assess the thermal resistance of the device with quite good reliability in the case of small lag effects.
On test bench, two different measurements have been performed to extract the thermal behaviour at 5W dissipated power:

- *CW* measurements with enclosure temperature equal to 25°C
- Pulsed measurements with enclosure temperature equal to 70°C

$$\Delta T = T_{junction_continuous\ mod\ e} - T_{enclosure} = R_{th} \times P_{diss} \ \ then\ \ T_{junction_continuous\ mod\ e} = 25°C + R_{th} \times P_{diss}$$

$$\Delta T = T_{junction_pulsed\ mod\ e} - T_{enclosure} = R_{th} \times P_{diss}$$

At the intersect point the junction's temperatures are equal then:

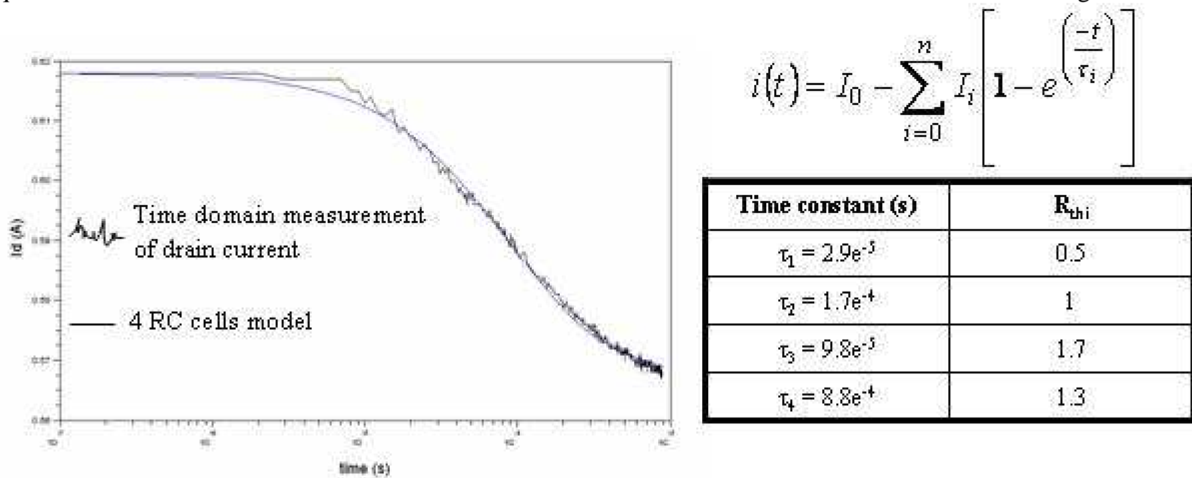
$$R_{th} = \frac{T_{junction_pulse} - T_{enclosure_continuous}}{P_{diss}}$$

$$R_{th} = 9°C / W$$

Thermal time constant

The principle of the determination of the thermal time constants is based in observing the current behavior within a quite large heating pulse. Such a large pulse enable to observe the different time-constants of the self-heating linked to the different materials constituting the active device.
In order to illustrate the different existing time constants related to the device technology, we visualize the shape of the current pulse through the transistor assuming that the supplied pulse is large enough.
A 1 ms duration pulse representing steady-state conditions. with 9V peak voltage is used during self-heating measurement test while device operating at 0V gate bias voltage and pulse manages drain voltage, leading to minimum lag effects.

A modeling circuit made of different parallel RC cells is a good way to electrically describe the temperature variation during time. Each parallel RC cell provides its own time constant. The Fig.6 shows the measured drop of the drain current at 5W dissipated power trough a 1 ms width pulse. In this case, a modeling circuit integrating 4 RC cells was required to match the measured data. Values of the extracted time constants are detailed in the following table.



$$i(t) = I_0 - \sum_{i=0}^{n} I_i \left[1 - e^{\left(\frac{-t}{\tau_i}\right)} \right]$$

Time constant (s)	R_{thi}
$\tau_1 = 2.9e^{-5}$	0.5
$\tau_2 = 1.7e^{-4}$	1
$\tau_3 = 9.8e^{-5}$	1.7
$\tau_4 = 8.8e^{-4}$	1.3

Figure 6 : Time domain comparison of measured and modeled drain current variation versus time through a 1ms width pulse at 29°C room temperature for 5W dissipated power.

LOAD PULL VALIDATION

At the end of the non linear modeling process, load pull measurements have been performed at the selected bias point *(100mA, 50V)* at 2.185GHz frequency. The Smith diagram on Fig.7 shows the comparison between measured and simulated areas of load impedances corresponding to *PAE* and Power contours. Crosses stand for measurement and solid lines for simulation. The maximum of measured *PAE* (power added efficiency) was found at Z_{load}=5.99+j14.25 Ω while the simulated one is Z_{load}=5.98+j14.35 Ω. Such a comparison enables to conclude on the very good model agreement at large signal power levels.

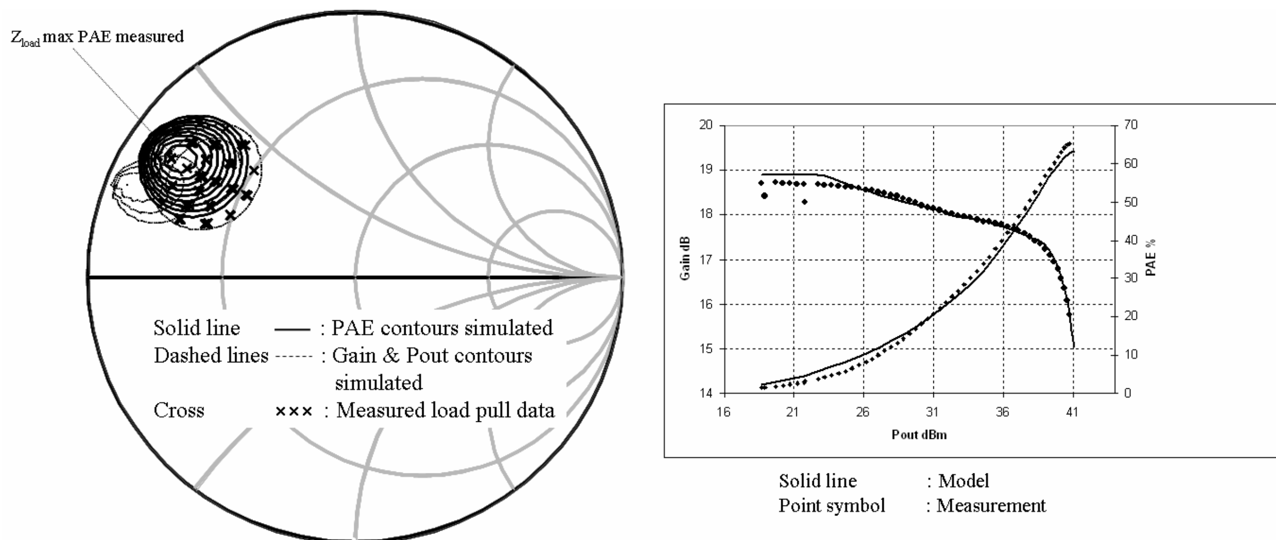


Figure 7 : Simulated and measured load pull data at (Id=100mA, Vd=50V) bias point and 2.185 GHz frequency.

The plotted curve at the right-hand side of Fig.7 makes a comparison of simulated and measured data at Z_{load} corresponding to the maximum measured *PAE* (i.e Z_{load} = 5.99+j14.25 Ω) at fundamental frequency, assuming that second and third harmonics are tuned to be equal to those of measurement (i.e $Z_{load@H2\ (4.37GHz)}$ = 8.3+j26.5 Ω and $Z_{load@H3\ (6.55GHz)}$ = 8.2+j20.4 Ω). It can be observed a very good agreement between modeled and measured behaviour from small signal up to 3dB power compression.

CONCLUSION

The presented modelling process enables to derive an accurate non linear electrothermal model (not including trapping effects [6]) of the high power packaged *GaN HEMTs* from 0.5 to 8GHz. On the one hand, the non linear model has been validated by checking its agreement with measured data from small signal operation (S-parameters) up to very high power operation (load-pull measurements). On the other hand, the selected topology and non linearity equations ensure a high convergence level for designer requirements particularly near to saturation.
In this paper, we have reported the development of an accurate electro-thermal model of *GaN* packaged power transistor in order to make a future smart design whose accuracy will mainly depend on the model reliability. The future design work should confirm the reliability of the current model and show his ability to work with a dynamic supply voltage environment.

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