System Modeling and Measurement for High Accuracy Verification

December 1st - 4th, 2009, Broomfield/Boulder, Colorado
OUTLINE

PART I : Pulsed IV and S parameters for GaN HEMT compact models
presented by T. Reveyrand (XLIM)

PART II : Load Pull Measurement setups
presented by T. Gasseling (AMCAD Engineering)
PART I : Pulsed IV and S parameters for GaN HEMT compact models

T. Reveyrand (XLIM)
Pulsed IV measurement system
for
GaN HEMT compact modeling
Instrumentation

(Pulsed) Load-Pull measurement setup

Compact modeling activities

Pulsed IV & [S] measurement setup (incl. Thermo-chuck)

Commercially available tools through the independent company **AMCAD Engineering**
Agilent Channel Partner – PNA-X based setups

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Pulsed S parameters

RF small signal

Vds(t)

Vds

Vds_i

Vds_o

0

0

10 μs

500 ns

550 ns

200 ns

250 ns

freq (4.000GHz to 40.00GHz)

dB(S(2,1))

freq, GHz

0

10

20

30

40

0

10

20

30

40

0

10

20

30

40

freq (4.000GHz to 40.00GHz)

phase(S(2,1))

freq, GHz

-arcsin-

phase(S(1,1))

freq, GHz

-arcsin-

phase(S(2,2))

freq, GHz

-arcsin-
Pulsed S parameters

Lag identification

Intrinsic parameters extraction
Commercially available system from AMCAD Engineering
Pulsed I(V) and S2P measurements

Dynamic measurements from a quiescent bias point

For each pulsed bias point, the complete S2P parameters (0.04-40GHz) are recorded

- 0.5 – 40 GHz
- 10A/240V
- 200 ns to 1 ms pulses
- -65 to 200 °C
Pulsed IV measurement system for GaN HEMT compact modeling
Frequency dependant elements extraction

- Set of extrinsics parameters
- Measured [S] parameters
- De-embedding
- Intrinsic parameters calculus from intrinsic admittance matrix

Simulated Annealing Optimization

\[ G_d = \text{Re}\{Y_{12}\} + \text{Re}\{Y_{22}\} \]
\[ G_m = \sqrt{A^2 + B^2 \left(1 + R_i^2 C_{gs}^2 \omega^2\right)} \]
\[ R_{gd} = \frac{- (\text{Re}\{Y_{12}\} + G_{gd})}{C_{gd}^2 \omega^2} \left[1 + \left(\frac{\text{Re}\{Y_{12}\} + G_{gd}}{\text{Im}\{Y_{12}\}}\right)^2\right] \]

... No

Fit ?

Yes

Linear Model Extraction

First step of Nonlinear Model Extraction

COMPLETED
Non-linear Model Extraction

Modeling process

Small Signal Model

I-V Model

Nonlinear capacitances

Thermal model

Trapping effects

Rs=f(T)

Rd=f(T)

Rgd=f(T)

Ids=f(Vgs,Vds,T)

Cgs=f(Vgs)

Cgd=f(Vgd)

Dgs=f(Vgs)

Dgd=f(Vgd)

Dgs=f(Vgs)

Dgd=f(Vgd)

Ids=f(Vgs,Vds,T)

Ids=f(Vgs_trap,Vds,T)
Modeling IV curves

\[ I_{d_{T_{ajima}}} = \frac{I_{DSS}}{1-\frac{1}{m}(1-e^{-m})} \left[ V_{GSN} - \frac{1}{m} \left(1-e^{-mV_{GSN}}\right) \right] \times \left[1-e^{-V_{DSS}(1-aV_{DSS}-bV_{DSS}^2)}\right] \]

\[ V_{GSN} = 1 + \frac{V_{GS}(t-\tau)-V\phi}{V_P} \]
Capacitances

Cgs et Cgd extracted from [S] parameters along the optimal load-line

\( C_{gs} = f(V_{gs}) \)

\( C_{gd} = f(V_{gd}) \)

Equations

\[
C_{gs} = C_0 + (C_1 - C_0) \cdot (0.5 + 0.5 \cdot \tanh(a \cdot (V_{gs} + V_m))) - C_2 \cdot (0.5 + 0.5 \cdot \tanh(b \cdot (V_{gs} + V_p)))
\]

Quiescent bias point

Load-line for Cgs and Cgd extraction

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Non-linear Models for designers

Classical Non-linear Model

- **Linear element**
- **Nonlinear element**
Non-linear Models for designers
Thermal effect Modelling

Thermal Simulations

Self Heating Extraction = f(t)

Exponential expansion:

\[ \text{TEMP} = 22.8 \cdot (1-e^{-t/t_1}) + 21.7 \cdot (1-e^{-t/t_2}) + 7 \cdot (1-e^{-t/t_3}) + \ldots \]
**Thermal effect Modelling**

**IV Modeling @ several temperatures**

**Measure / IV Model @ 25°C**

**Measure / IV Model @ 150°C**

**IV parameters versus temperature**

**Equations**

Thermal parameters
- Access Resistances
- Current Source
- Diodes

\[ R_s = R_{s0} + \alpha_{R_s} \cdot T \]
\[ R_d = R_{d0} + \alpha_{R_d} \cdot T \]
\[ I_{dss} = I_{dss0} + I_{dss1} \cdot T \]
\[ P = P_0 + P_1 \cdot T \]
\[ N_{gs} = N_{gs0} + N_{gs1} \cdot T \]
\[ N_{gd} = N_{gd0} + N_{gd1} \cdot T \]
\[ I_{ssg} = I_{ssg0} + I_{ssg1} \cdot e^{(T/T_{ssg})} \]
\[ I_{sgd} = I_{sgd0} + I_{sgd1} \cdot e^{(T/T_{sgd})} \]
IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 55, NO. 9, SEPTEMBER 2007

Self-Consistent Electrothermal Modeling of Class A, AB, and B Power GaN HEMTs Under Modulated RF Excitation

Vittorio Camarchia, Member, IEEE, Federica Cappelluti, Member, IEEE, Marco Pirola, Member, IEEE, Simona Donati Guerrieri, Member, IEEE, and Giovanni Ghione, Fellow, IEEE
Trapping effect Modelling

Gate- and drain-lag model topology (for ONE trap)

- Trapping effect on the current modeled with a modification of the control voltage (= Vgs)
  - Creates transients on Vgs = Current transients
  - Charging state of the capacitance = charging state of the traps
  - Fills through $R_{\text{capture}}$, releases through $R_{\text{remission}}$

Fills and releases model of traps (diode)

Processing: null offset, current dependencies, etc.

**Fundamental effect**: fill / release trapping time constants are different

- modeled with an envelope detector

  - Circuits number = Modeled traps number
  - 3 parameters to extract per circuit: $R_{\text{capture}}$, $R_{\text{release}}$, $k$
Trapping effect Modelling

Trap model parameters extraction

Current transient measurement, Negative pulse on Vds (emission)

- numbers of traps
- emission time constants
- relative amplitude of each trap

Avoid thermal effects during measurement

ONLY ONE MEASUREMENT TO OBTAIN ALL THOSE PARAMETERS
Model Validity: Large Signal Measurements @ power optimal load impedance

- Traps ON
- Traps OFF
- Measurements

Graphs showing:
- PAE(%) vs. Pin (dBm)
- IDS (mA) vs. Pin (dBm)
- Gain (dB) vs. Pin (dBm)
- Pout (W) vs. Pin (dBm)
- Mag (Gamma_in) vs. Pin (dBm)

Graphs indicate the comparison between model predictions and measurements for various parameters under different conditions.
The current slope phenomenon
The current slope phenomenon

Charging state of the traps (Drain-lag)
The current slope phenomenon

Charging state of the traps (Drain-lag)
The current slope phenomenon

Charging state of the traps (Drain-lag)

Saturation = Auto-bias
Completed Nonlinear Model
An Electrothermal Model for AlGaN/GaN Power HEMTs Including Trapping Effects to Improve Large-Signal Simulation Results on High VSWR

Olivier Jardel, Fabien de Groote, Tibault Reveyrand, Jean-Claude Jacquet, Christophe Charbonniard, Jean-Pierre Teyssier, Didier Floriot, and Raymond Quéré, Senior Member, IEEE
PART II : Load Pull Measurement setups

T. Gasseling (AMCAD Engineering)
Load Pull for PA Design: LPPD

The needs
Existing architectures

Load Pull for Model Validation: LPMV

Specific needs
Measurement definition
Specific Architecture

News trends

Time domain measurements for model validation
Load Pull used for PA Design: LPPD

The needs

Existing architectures

Load Pull used for model validation: LPMV

Specific needs
Measurement definition
Specific Architecture

News trends

Time domain measurements for model validation
**Load Pull for PA Design**

**The needs:**

- From the target definition (Pout, Efficiency, Gain etc.)

- **Power performances versus Zsource and Z load**

- **ISO-circles plot -> Determination of optimal operating conditions**

- **Transistor performances evaluation associated to given operating conditions for the design of PA.**

- **Transistor model validation**
**Load Pull for PA Design**

*LPPD architecture*

The LPPD setups have been developed in order to find the transistor’s optimal source and load impedances for defined and fixed operating conditions.
These **LPPDs** setups can be used for:

Transistor performances evaluation for given operating conditions (transistor + setup combination)

Determination of optimal load impedances: useful for PA design when nonlinear models are not available

These **LPPDs** setups cannot be used for:

A determination of the intrinsic transistor characteristics useful for transistor model validation.
Can a **LPPD** setup measure Power Added Efficiency?

**The answer is: NO.** A passive load pull system measures the source power (available) toward the input of the DUT and the power delivered by the DUT to the load.

If a directional coupler is used to measure the power returned by the DUT to the source, in order to assess the really absorbed power by the DUT, then the loss of the input tuner and the coupler can only be calculated if we know the large signal input impedance of the DUT.

**However:** If the **DUT is perfectly input matched** and only then, the Efficiency measured equals the Power Added Efficiency defined as:

\[
PAE = \frac{\text{Power delivered to load} - \text{Power delivered to DUT}}{\text{DC power}};
\]

and the Gain measured becomes Power Gain

\[
Gp = \frac{\text{Pout-del}}{\text{Pin-del}}
\]

But one has to be careful: If the DUT is tuned at the input so that the reflected power to the source (measured via the 4th port of the input coupler or the third port of a circulator) becomes zero, **this does not mean** the DUT is "input matched", it means that the setup is matched at the intersection between tuner and circulator, not tuner and DUT.
Illustration: Measurements on a FET @ f0=4GHz

Illustration showing a microwave measurement setup with a Power Amplifier, Input Coupler, DUT, Power Meter, and S11, S22 parameters.
Illustration: Measurements on a FET @ f_0=4GHz
Illustration: Measurements on a FET @ f0=4GHz

The source tuner is matched (not the DUT)
Illustration: Measurements on a FET @ f0=4GHz

The DUT is matched (not the source tuner)
Can a PA Load Pull System measure Power Added Efficiency? : The answer is: NO.

The assumption that the Efficiency measured equals the Power Added Efficiency only when the “DUT is input matched” and only then, means that this assumption is valid only when the source pull optimization (iso-Pout or Gain circles) is done for a constant amount of input power injected into the DUT.

As a consequence, because the transistor’s input impedance is related to the amount of power injected in the DUT, this optimization must be done for each power level.
Conclusion:

Each time the power injected in the DUT is varied, the transistor input impedance is varied as well, and then the assumption of the perfect matching at the input could not be done any more.

If the transistor’s intrinsic PAE needs to be measured, then the source impedance should be optimized for each power step: cumbersome and time consuming.

Ordinary load pull architecture are useful for PA designers but raw data such as gain and Efficiency measurements are not accurate enough to be used for model validation.
Conclusion:

In addition, measurements made with power meters are mean power measurements.

When in the bandwidth of the power sensor, the power measured corresponds to the power generated at the fundamental and harmonic frequencies.

For model validation, the wanted power (at the fundamental frequency) and the power generated at harmonic frequencies, should be measured independently.
Some LPPDs setups have been updated in order to measure the transistor’s input reflection coefficient:
Some LPPDs setups have been updated in order to measure the transistor’s input reflection coefficient:

- The lower Zin-DUT
- The Higher src tuner losses
- The lower the input deembedding accuracy

Problem: The transistor power gain is really sensitive to the $\Gamma_{in}$ meas accuracy.
Illustration: Gin measurements / LPPD setups

Source pull: for each source impedance, the Gin measurement is de-embedded through a new input tuner’s set of S2P bloc file.

While the measurement accuracy if data such as $P_{out}$ or Transducer Power gain versus $Z_{source}$ are convenient for PA design.
Illustration: Gin measurements / LPPD setups

Source pull: for each source impedance, the Gin measurement is de-embedded through a new input tuner’s set of S2P bloc file.

Some of them such as |Γin| or power gain are not accurate enough for Model validation.
Load Pull used for PA Design: LPPD

The needs

Existing architectures

Load Pull used for Model Validation: LPMV

Specific needs

Measurement definition

Specific Architecture

News trends

Time domain measurements for model validation
Load Pull used for Model Validation

Specific needs

Measurement of the transistor input impedance, whatever the operating conditions (Zload, Power level etc.)

Narrow band measurements at f0, 2f0, 3f0 etc.

True calculus of $\Gamma_{in}$, PAE, Gain ...

Transistor model validation
Load Pull used for model validation

Measurement definition

\( P_{\text{in}} \): Power delivered to the DUT by the source

\[
P_{\text{in}} = \frac{1}{2} (|u1|^2 - |b1|^2) = \frac{1}{2} |u1|^2 (1 - |\Gamma_{\text{in}}|^2)
\]

\( P_{\text{source}} \): Power delivered by the source

\[
P_{\text{source}} = \frac{P_{\text{in}}}{1 - |\frac{Z_{\text{in}} - Z_{\text{source}}}{Z_{\text{in}} + Z_{\text{source}}}|^2}
\]

\( P_{\text{out}} \): Power delivered to the load impedance

\[
P_{\text{out}} = \frac{1}{2} (|b2|^2 - |a2|^2) = \frac{1}{2} |b2|^2 (1 - |\Gamma_{\text{load}}|^2)
\]
Load Pull used for model validation

**Measurement definition**

**Power gain** is the ratio of the power delivered to the load \( P_{\text{out}} \) to the power delivered to the transistor by the source \( P_{\text{in}} \).

\[
\text{Gain}^{\text{Power}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{|b2|^2(1 - |\text{Load}|^2)}{|a1|^2(1 - |\text{In}|^2)}
\]

**Transducer Power gain** is the ratio of the power delivered to the load \( P_{\text{out}} \) to the power available from the source \( P_{\text{source}} \).

\[
\text{Gain}^{\text{trans}} = \frac{P_{\text{out}}}{P_{\text{source}}} = \frac{|b2|^2(1 - |\text{Load}|^2)}{|a1|^2(1 - |\text{In}|^2)} \ast \left(1 - \left|\frac{\text{Zin} - \text{Zsource}}{\text{Zin} + \text{Zsource}}\right|^2\right)
\]

\[
\text{Gain}^{\text{Power}} = \text{Gain}^{\text{trans}} \text{ if } \text{Zin} = \text{Zsource} \ast
\]
Load Pull used for model validation

**Measurement definition**

**Power added Efficiency** is the ratio of the power added by the transistor to the power consumed.

\[
PAE = \frac{(P_{out} - P_{in})}{P_{DC}} \times 100\%
\]

**Transducer Efficiency** is the ratio of the power added by the source + transistor to the power consumed.

\[
Eff = \frac{(P_{out} - P_{source})}{P_{DC}} \times 100\%
\]

\[
PAE = Eff \quad \text{if} \quad Z_{in} = Z_{source} *
\]
Load Pull used for model validation

Measurement definition

**Power added Efficiency** is the ratio of the power added by the transistor to the power consumed.

\[
\text{PAE} = \frac{(P_{\text{out}} - P_{\text{in}})}{P_{\text{DC}}} \times 100\%
\]

**Transducer Efficiency** is the ratio of the power added by the source + transistor to the power consumed.

\[
\text{Eff} = \frac{(P_{\text{out}} - P_{\text{source}})}{P_{\text{DC}}} \times 100\%
\]

\[
\text{PAE} = \text{Eff} \text{ if } Z_{\text{in}} = Z_{\text{source}} *
\]
Illustration: Measurements on a FET @ f0=4GHz

Used for model validation

Power gain

- Max power gain (dB) @ f0
- Pin min (dBm) @ f0

Used for PA design

Transducer Power gain

- Transducer Power gain (dB)
- Pin min (dBm) @ f0

Measurements done on the same transistor
Illustration: Measurements on a FET @ f0=4GHz

Used for PA design

Transducer Power gain

Gamma in [Real] @ f0

Gamma in [Imaginary] @ f0

-0.65 -0.6 -0.55 -0.5 -0.45 -0.4 -0.35 -0.3 -0.25 -0.2 -0.15 -0.1 -0.05 0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4

-1.0 -0.95 -0.9 -0.85 -0.8 -0.75 -0.7 -0.65 -0.6 -0.55

Zsource1
-5.88 + 14.796i ohms

Zsource2
6.334 + 8.365i ohms

Zsource3
11.95 + 12.083i ohms

Transducer Power gain (dB) [f0]

-20.0 -17.5 -15.0 -12.5 -10.0 -7.5 -5.0 -2.5 0.0 2.5 5.0 7.5 10.0 12.5 15.0 17.5 20.0

Pin min (dEm) [f0]
Illustration: Measurements on a FET @ f0=4GHz

Used for model validation

**PAE**

![Plot of PAE vs Pin (dBm)]

-30.0, -25.0, -20.0, -15.0, -10.0, -5.0, 0.0, 5.0, 10.0, 15.0 dBm

PAE (%)

0.0, 10.0, 20.0, 30.0, 40.0, 50.0, 60.0%

Used for PA design

**Transducer Efficiency**

![Plot of Efficiency vs Pin (dBm)]

-25.0, -20.0, -15.0, -10.0, -5.0, 0.0, 5.0, 10.0, 15.0, 20.0, 25.0 dBm

Efficiency (%)

0.0, 10.0, 20.0, 30.0, 40.0, 50.0, 60.0%

Zsource1: X: 10.214, Y: 53.009
Zsource2: X: 16.849, Y: 41.055
Zsource3: X: 8.683, Y: 27.606

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AMCAD Engineering
Load Pull used for model validation

Specific Architecture
Specific Architecture

- DC or pulse DC supplies + meas Units
- Low loss directional couplers
- CW or pulse RF signal f0 or f1+f2
- Tuner f0
- VNA
- Tuner f0, 2f0, 3f0
- Drain 50Ω

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Specific Architecture

AMCAD Load Pull system used for modelling activities
Conclusion

Model validation using load pull measurements: VNA use instead of power meters

- Measurement in narrow band mode = F0 meas. + 2F0 meas. Instead of mean power meas.
- Better dynamic range = better meas. Accuracy
- Vector measurement s instead of scalar measurements = useful data for model validation
News trends

*Time domain measurements for model validation*

*Time domain measurements for MMIC validation*
Characteristics of transistor used:

- $V_{BK} > 100V$
- $R_{dson} \approx 2 \text{ ohm}$
- $C_{ds} = 0.9 \text{ pF}$
- $C_{gs} = 8 \text{ pF}$
- $R_g = 0.5 \text{ ohm}$

**Device used:** 15 W GaN HEMT from CREE CGH60015D

**Device size:** 2mm
Measure

Simulation

Class E

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News trends

Time domain measurements for model validation

Time domain measurements for MMIC validation
Objective

Time domain Measurement Setup

MTA (Microwave Transition Analyser)
- Obsolete
- 2 channels

LSNA (Large Signal Network Analyser)
- Advanced technology (calibrated)
- 4 channels
- Commercially available

RF sampling scope
- Long acquisition time
- Time base distortions

MMIC
Configuration

HIP calibration assumption

Measurement Setup

\[ V_{\text{ref. plane}}(f) = \tilde{K}(f) \cdot V_{\text{raw}}(f) \]
Applications

IN OUT

Frequency LSNA Analysis Grid

2.15 GHz Fundamental + 8 harmonics

$V_{be} = 1V$

$V_{ce} = 9V$

Measurement setup

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