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ARFTG - Microwave Measurement Conference

System Modeling and Measurement for High Accuracy Verification

December 1st - 4th, 2009, Broomfield/Boulder, Colorado

AMCAD Engineering
Advanced Modeling for Computer-Aided Design

OUTLINE

PART I : Pulsed IV and S parameters for GaN HEMT compact models

presented by T. Reveyrand (XLIM)

PART II : Load Pull Measurement setups

presented by T. Gasseling (AMCAD Engineering)

PART I : Pulsed IV and S parameters for GaN HEMT compact models

T. Reveyrand (XLIM)

Pulsed IV measurement system
for
GaN HEMT compact modeling

Instrumentation

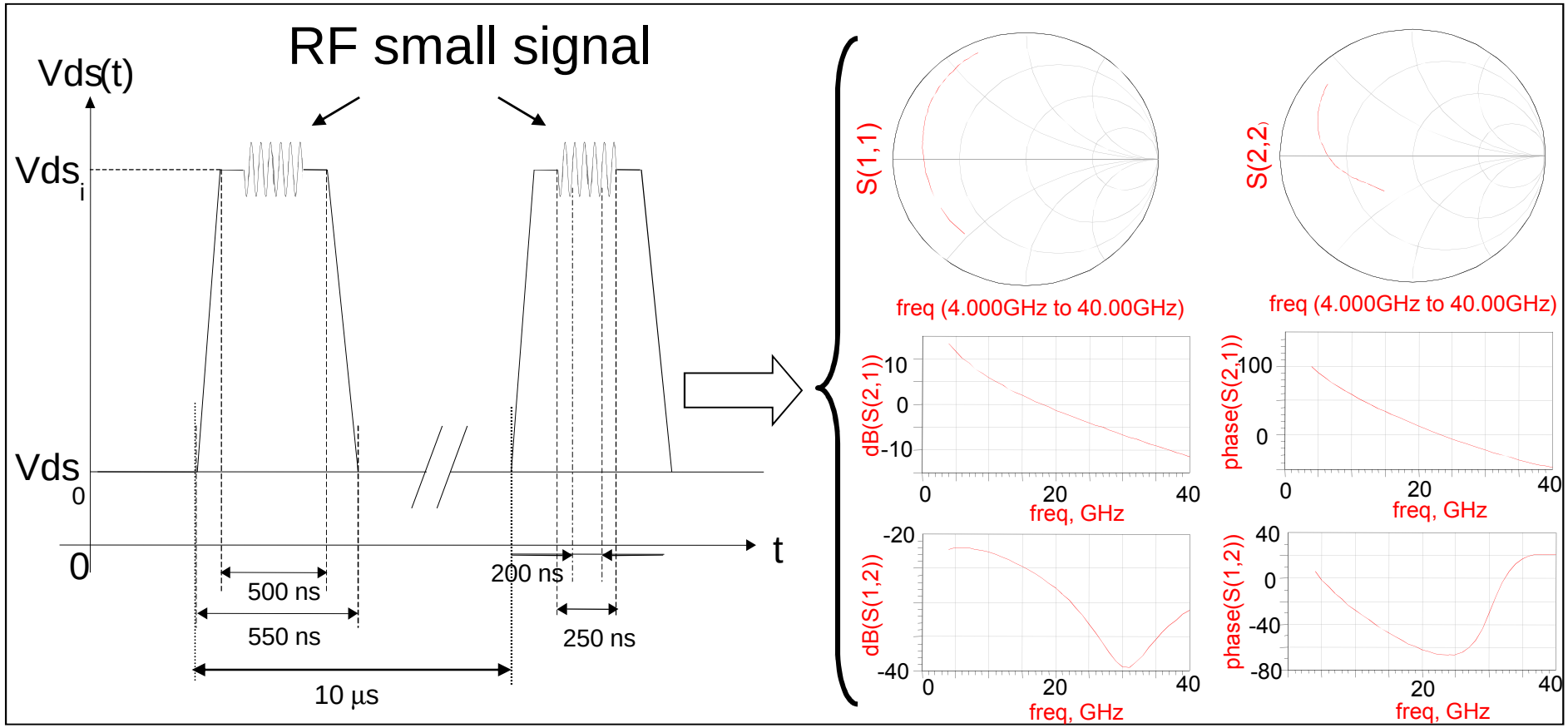
Compact modeling activities

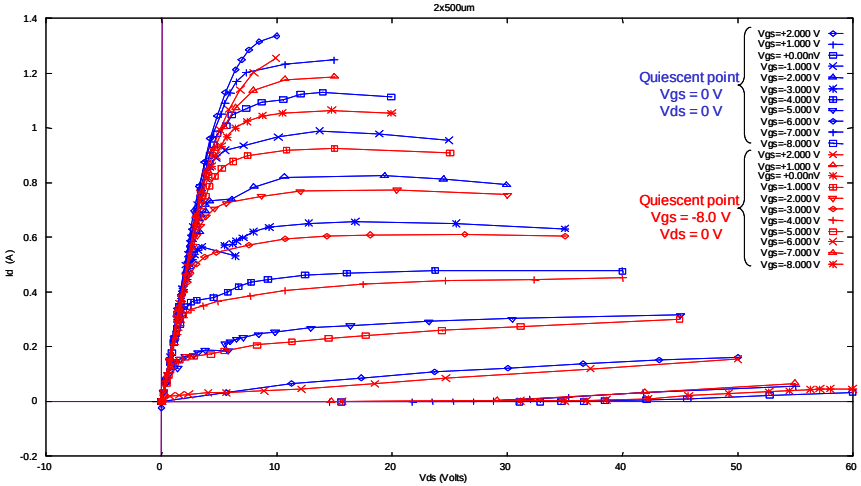
(Pulsed) Load-Pull measurement setup

Pulsed IV & [S] measurement setup
(incl. Thermo-chuck)

Commercially available tools through the independent company **AMCAD Engineering**
Agilent Channel Partner – PNA-X based setups

Pulsed S parameters

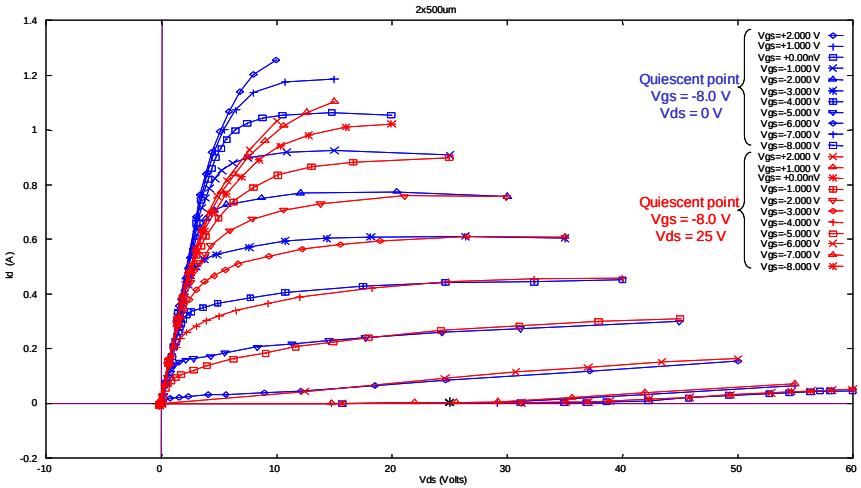


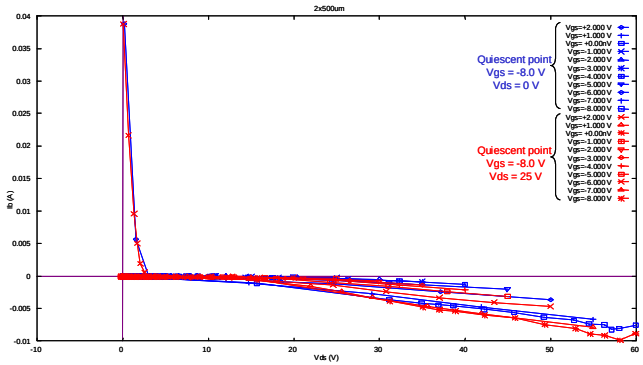


Pulsed S parameters

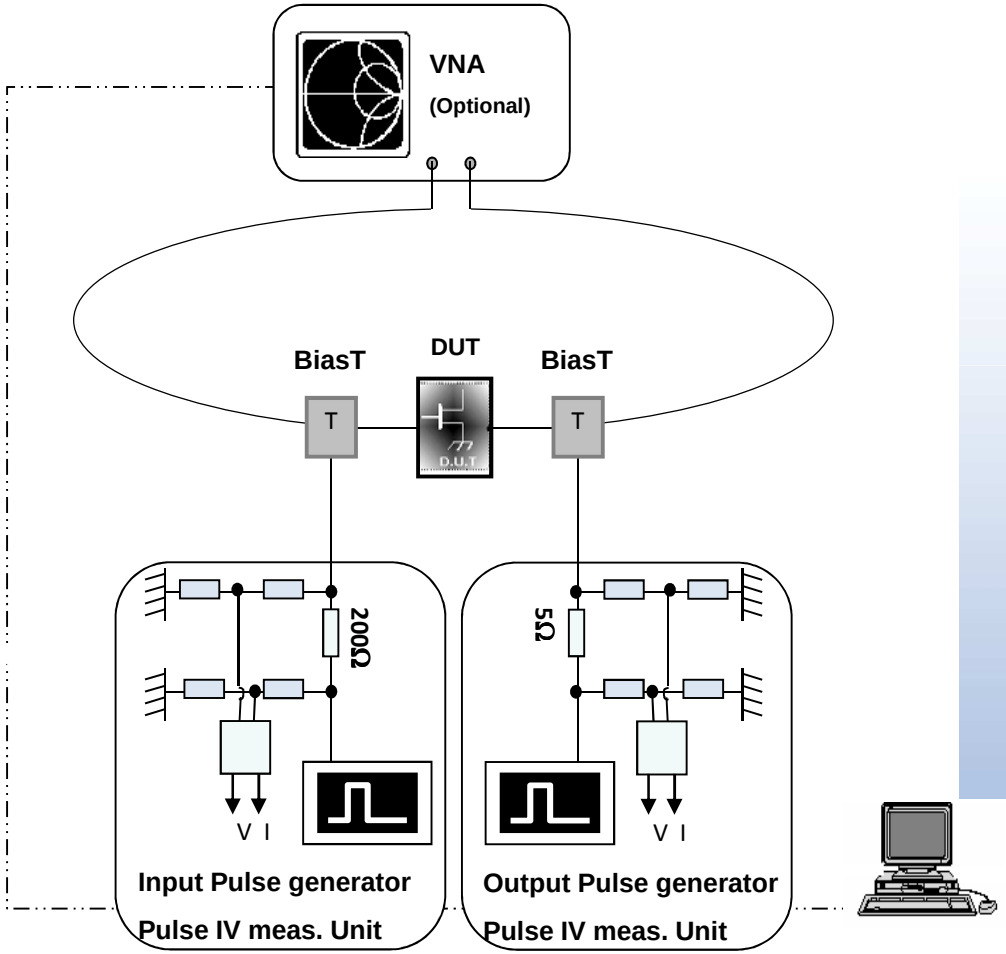
Lag identification

Intrinsic parameters extraction





Commercially available system from AMCAD Engineering



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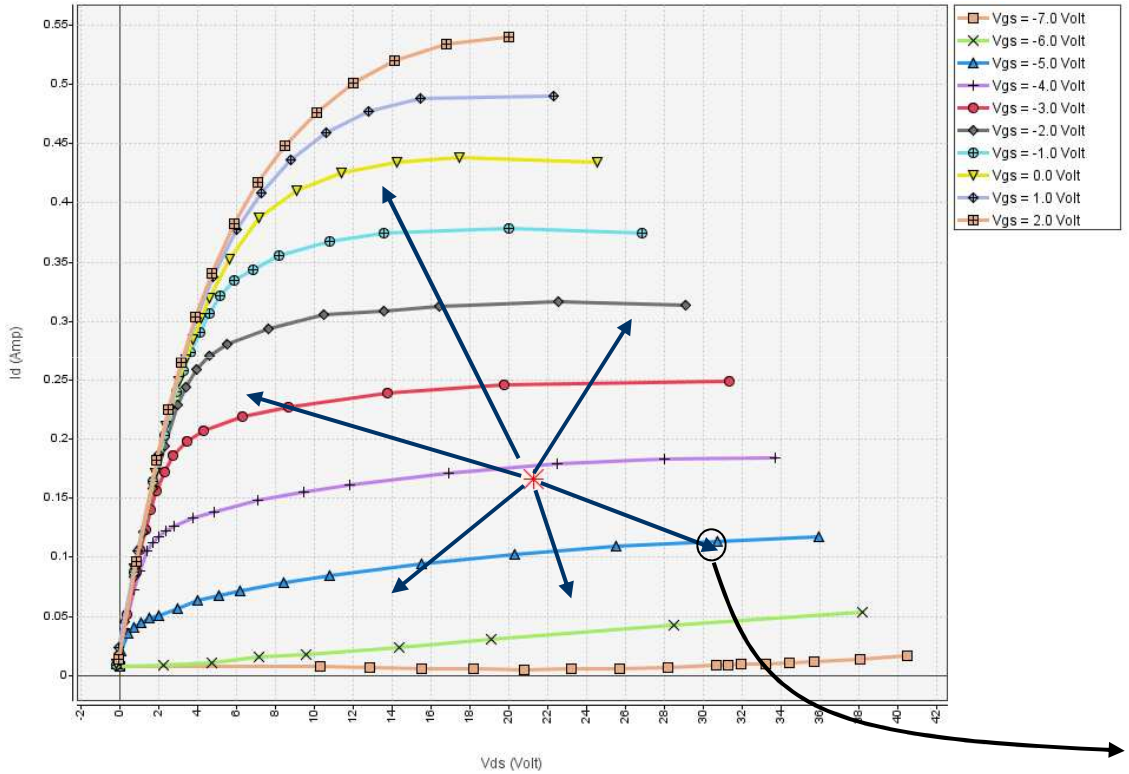
Pulsed I(V) and S2P measurements



Thermal chuck & Pulsed IV and S parameter measurement system used for model extraction

- **0.5 – 40 GHz**
- **10A/240V**
- **200 ns to 1 ms pulses**
- **- 65 to 200 °C**

Dynamic measurements from a quiescent bias point

For each pulsed bias point, the complete S2P parameters (0,04-40GHz) are recorded

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Pulsed IV measurement system for GaN HEMT compact modeling

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Linear Model Extraction

Frequency dependant elements extraction

Simulated Annealing Optimization

Set of extrinsics parameters

↓

Measured [S] parameters

↓

De-embedding

↓

Intrinsics parameters calculus from intrinsic admittance matrix

$$Gd = Re\{Y12\} + Re\{Y22\} \qquad Gm = \sqrt{\left(A^2 + B^2\right)\left(1 + Ri^2 Cgs^2 \omega^2\right)}$$

$$Rgd = \frac{-\left(Re\{Y12\} + Gdgd\right)}{Cgd^2 \omega^2}\left[1 + \left(\frac{Re\{Y12\} + Gdgd}{Im\{Y12\}}\right)^2\right]$$

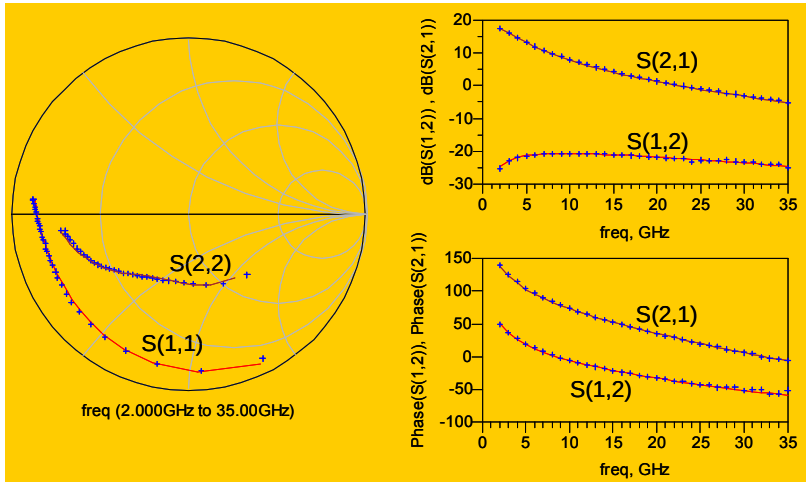
...

↓

Fit ?

No

Yes



First step of Nonlinear Model Extraction
COMPLETED

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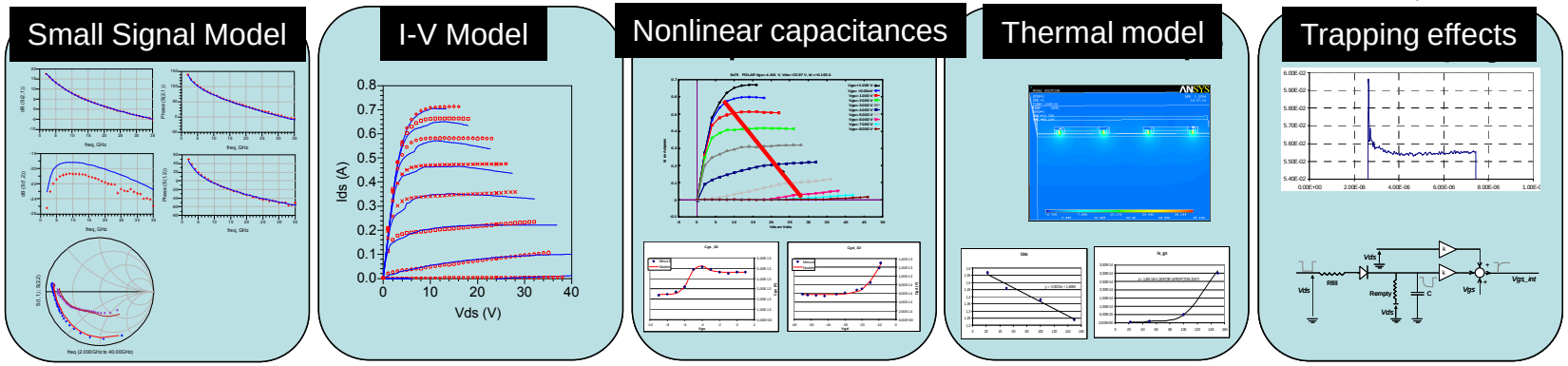
Non-linear Model Extraction

Modeling process



Rg
Lg
Cpg
Ls
Cpd
Ld
~~Rs~~
~~Rd~~

Ri
Cds
τ
~~Gm~~
~~Gd~~
~~Cgs~~
~~Cgd~~
~~Rgd~~

~~Dgs=f(Vgs)~~
~~Dgd=f(Vgd)~~
~~Ids=f(Vgs,Vds)~~

Cgs=f(Vgs)
Cgd=f(Vgd)

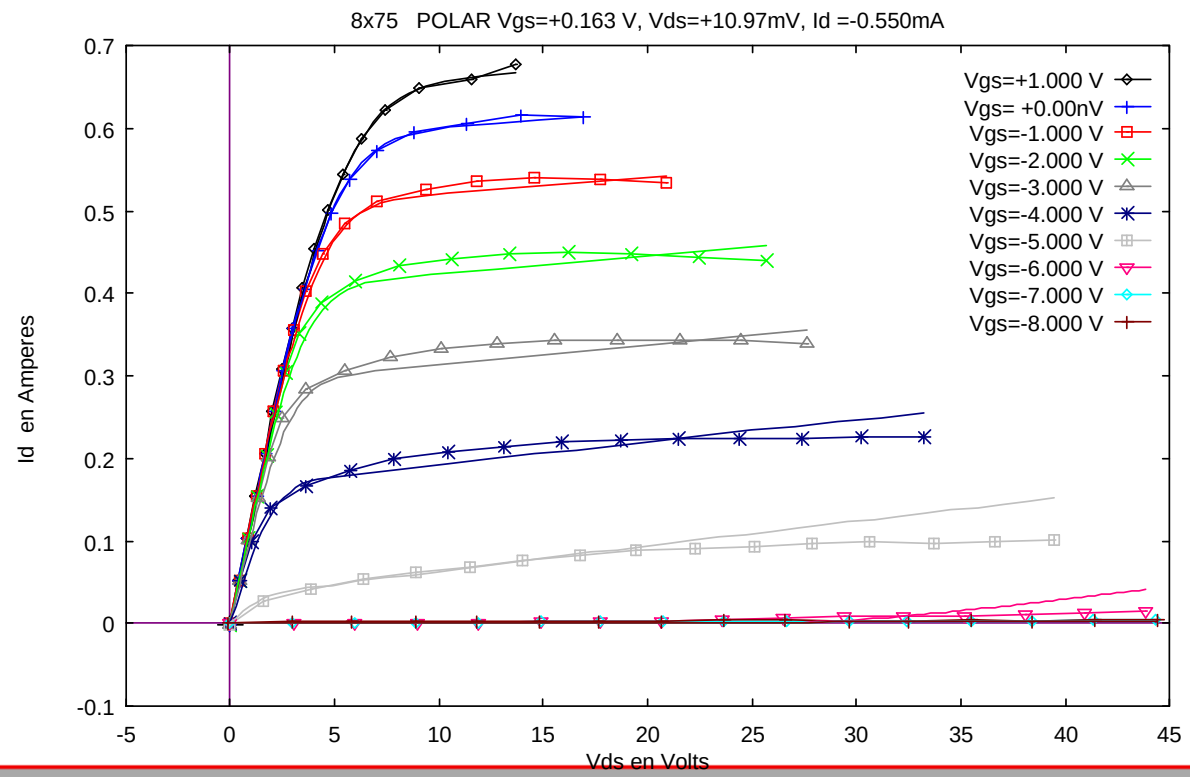
Rs=f(T)
Rd=f(T)
Rgd=f(T)

Dgs=f(Vgs)
Dgd=f(Vgd)
~~Ids=f(Vgs,Vds,T)~~ → Ids=f(Vgs_trap,Vds,T)

Modeling IV curves

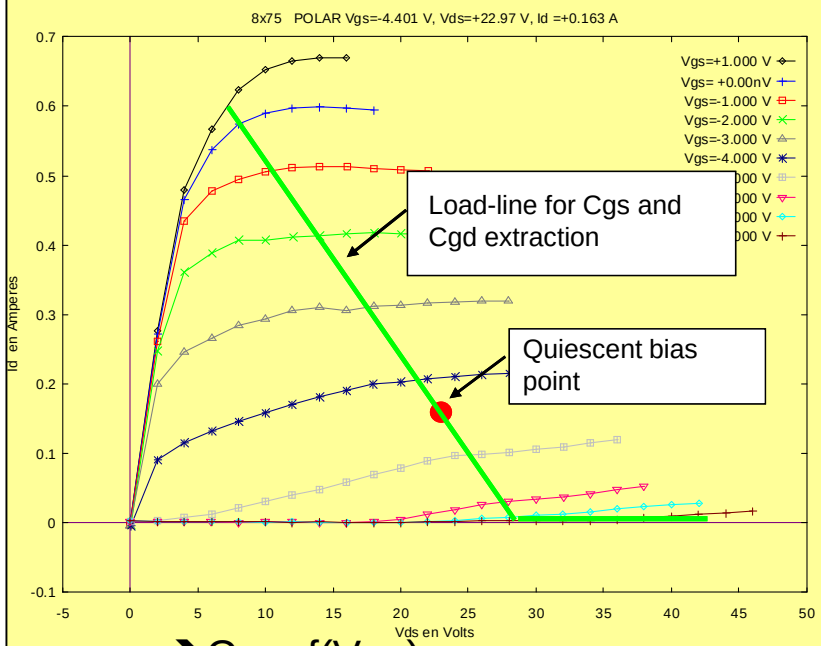
$$Id_{Tajima} = \frac{I_{DSS}}{1-\frac{1}{m}\left(1-e^{-mV_{GSN}}\right)}\left[V_{GSN}-\frac{1}{m}\left(1-e^{-mV_{GSN}}\right)\right]\times\left[1-e^{-V_{DSN}\left(1-aV_{DSN}-bV_{DSN}^{2}\right)}\right]$$

$$V_{GSN} = 1+\frac{V_{GS}(t-\tau)-V\phi}{V_P}$$



Capacitances

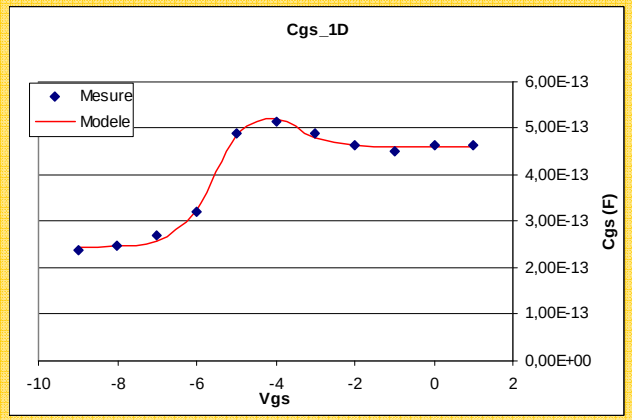
Cgs et Cgd extracted from [S] parameters along the optimal load-line

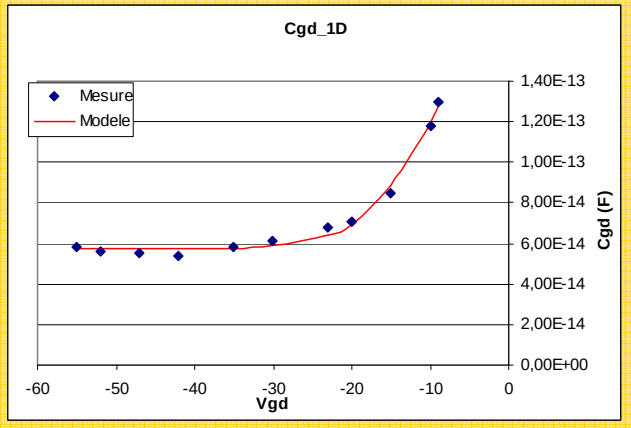


➔Cgs=f(Vgs)

➔Cgd=f(Vgd)

Equations





Cgs=C0+(C1-C0).(0,5+0,5.tanh(a.(Vgs+Vm)))

-C2.(0,5+0,5.tanh(b.(Vgs+Vp)))

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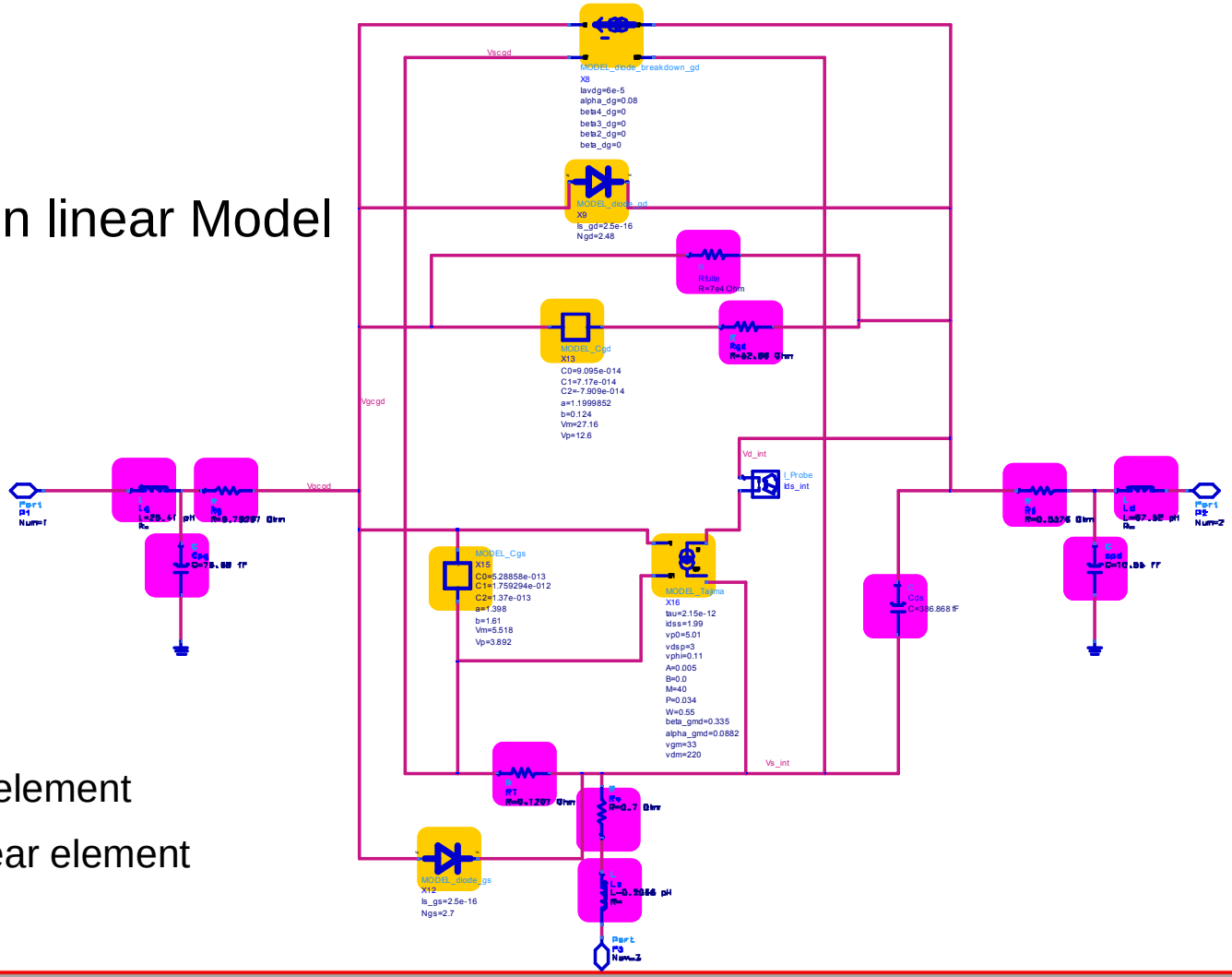
Non-linear Models for designers

Classical Non linear Model



Linear element

Nonlinear element

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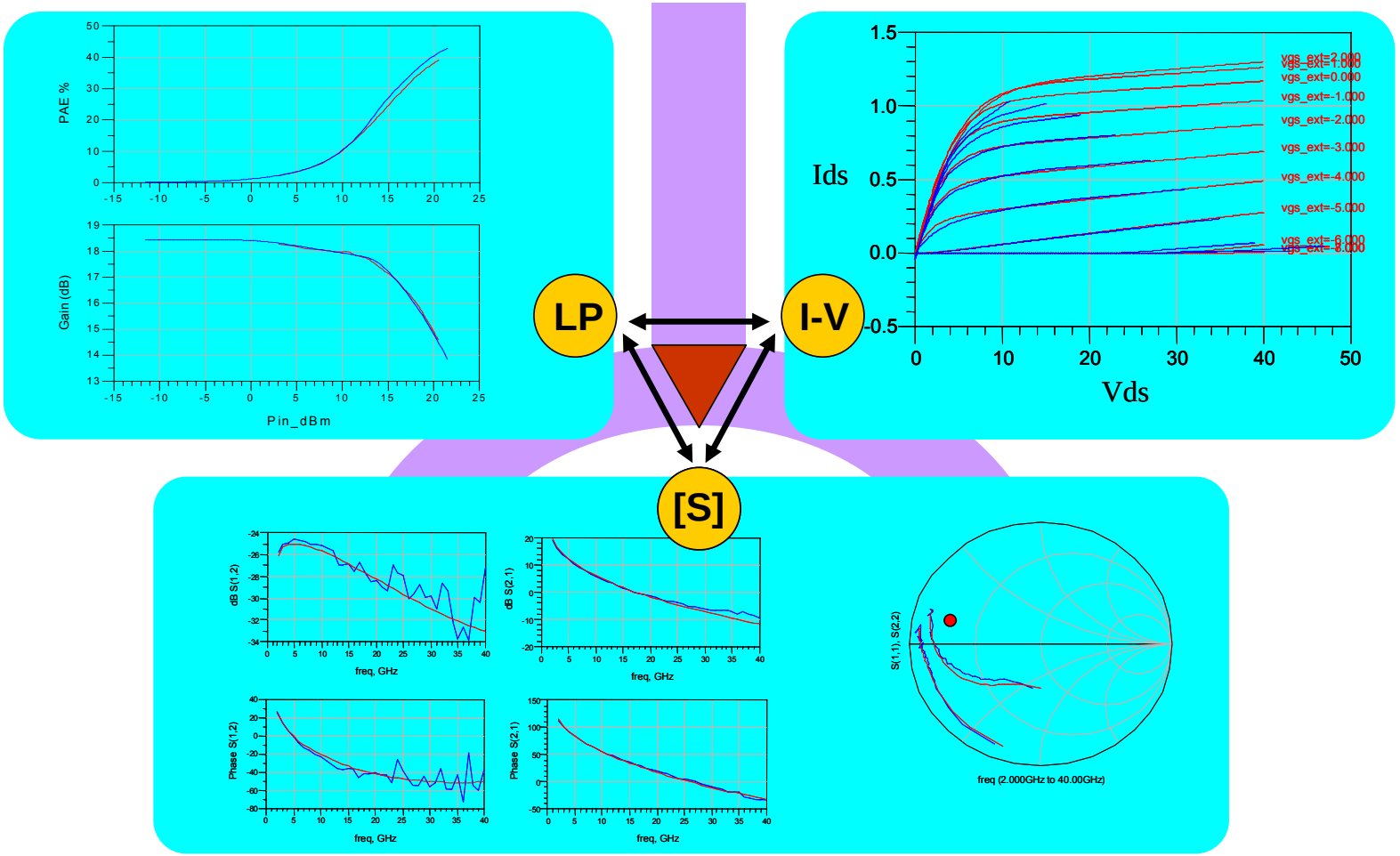
Non-linear Models for designers



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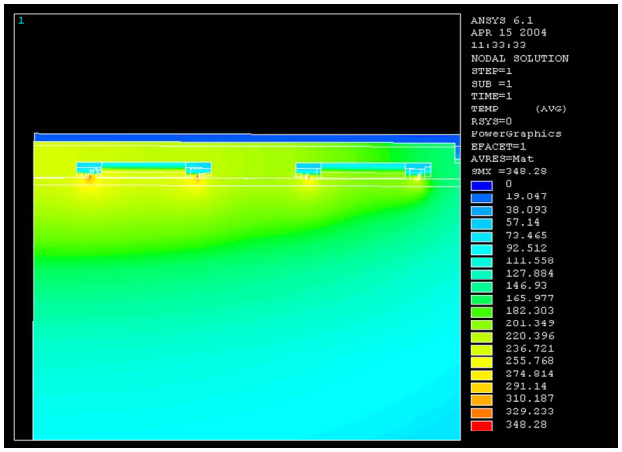
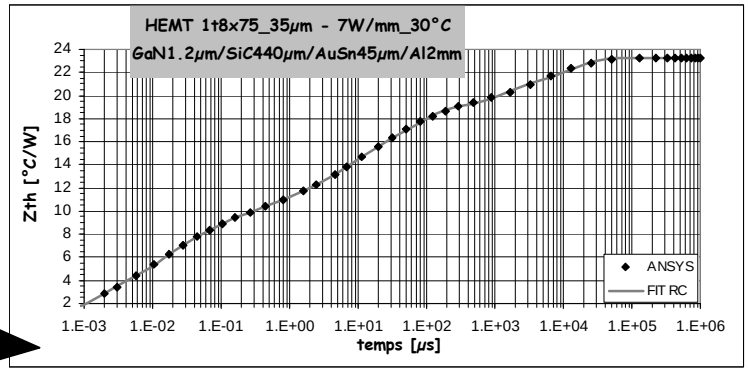
Thermal effect Modelling

Thermal Simulations



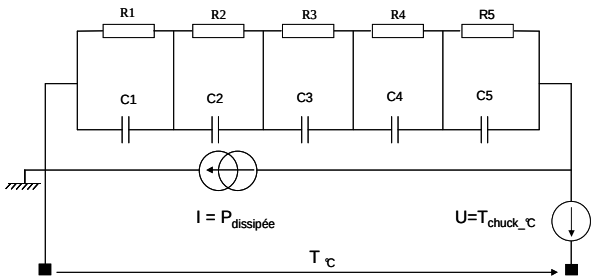
Self Heating Extraction = f(t)



Exponential expansion :

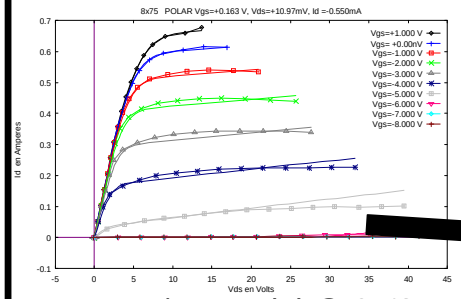
TEMP = 22,8.(1-e-t/τ1)
+ 21,7.(1-e-t/τ2)
+ 7.(1-e-t/τ3)
+ …

RC cells behavior

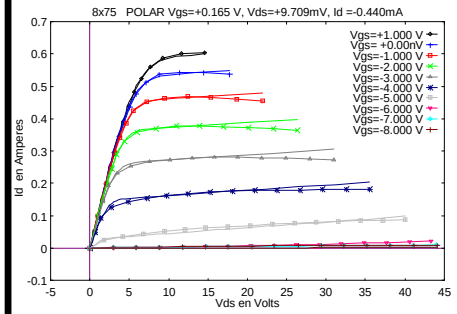


Thermal effect Modelling

IV Modeling @ several temperatures

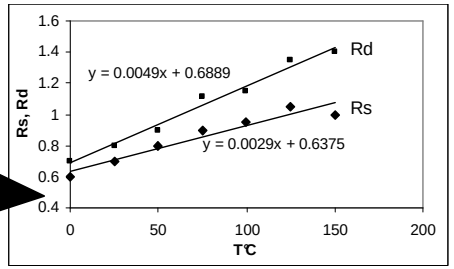


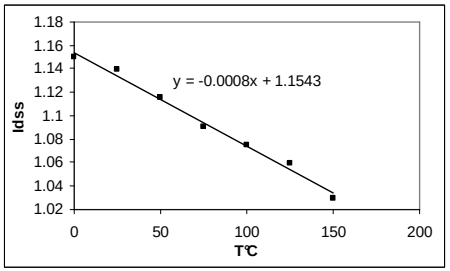
Measure / IV Model @ 25℃



Measure / IV Model @ 150℃

IV parameters versus temperature





Equations

Thermal parameters

- Access Resistances
- Current Source
- Diodes

$Rs = Rs_0 + \alpha\_Rs.T$

$Rd = Rd_0 + \alpha\_Rd.T$

$Idss = Idss_0 + Idss_t.T$

$P = P_0 + P_t.T$

$Ngs = Ngs_0 + Ngs_t.T$

$Ngd = Ngd_0 + Ngd_t.T$

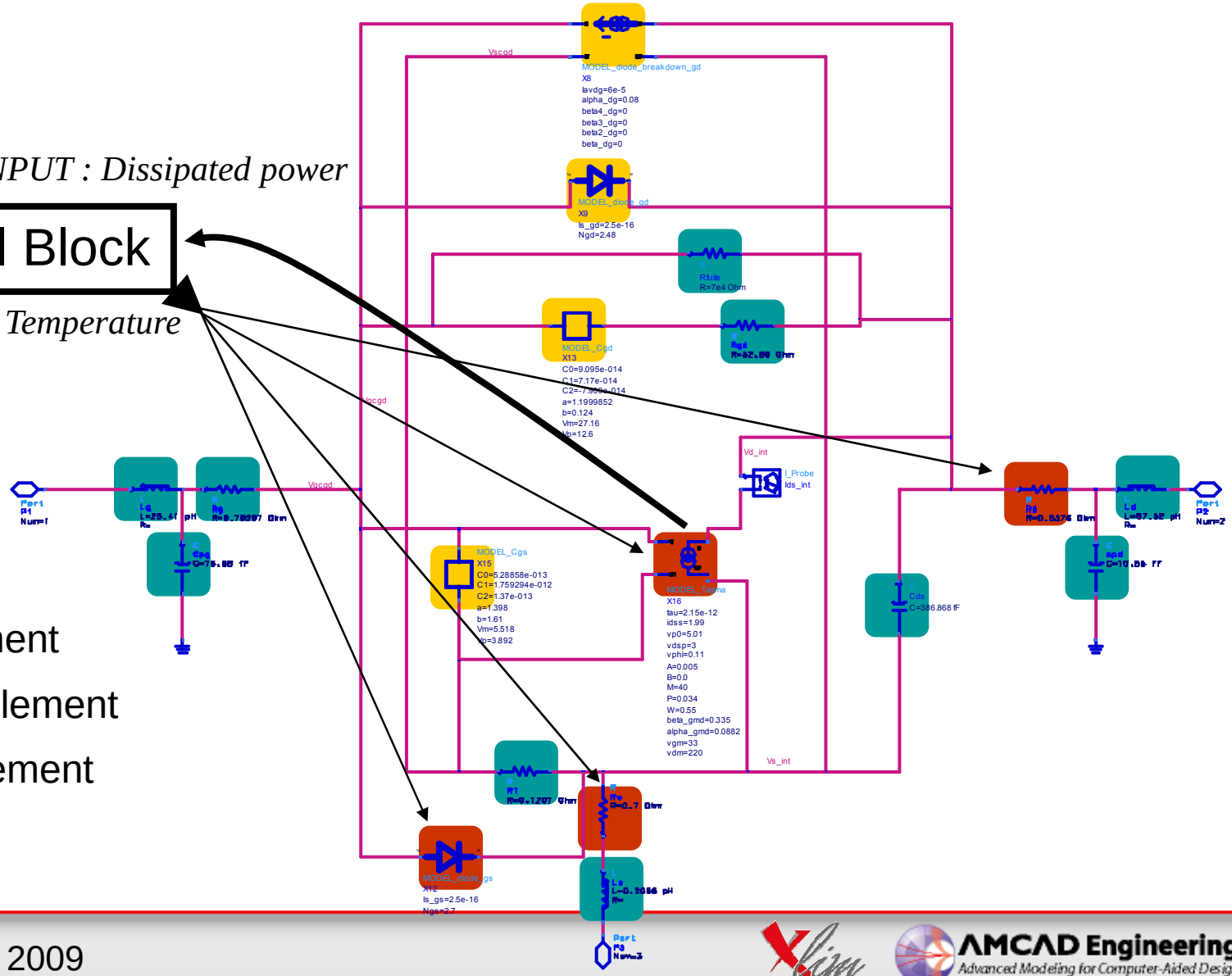
$Isgs = Isgs_0 + Isgs_t.e^{(T/Tsgs)}$

$Isgd = Isgd_0 + Isgd_t.e^{(T/Tsgd)}$

INPUT : Dissipated power

Thermal Block

OUTPUT : Temperature



Linear element

Nonlinear element

Thermal element

IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 55, NO. 9, SEPTEMBER 2007

Self-Consistent Electrothermal Modeling of Class A, AB, and B Power GaN HEMTs Under Modulated RF Excitation

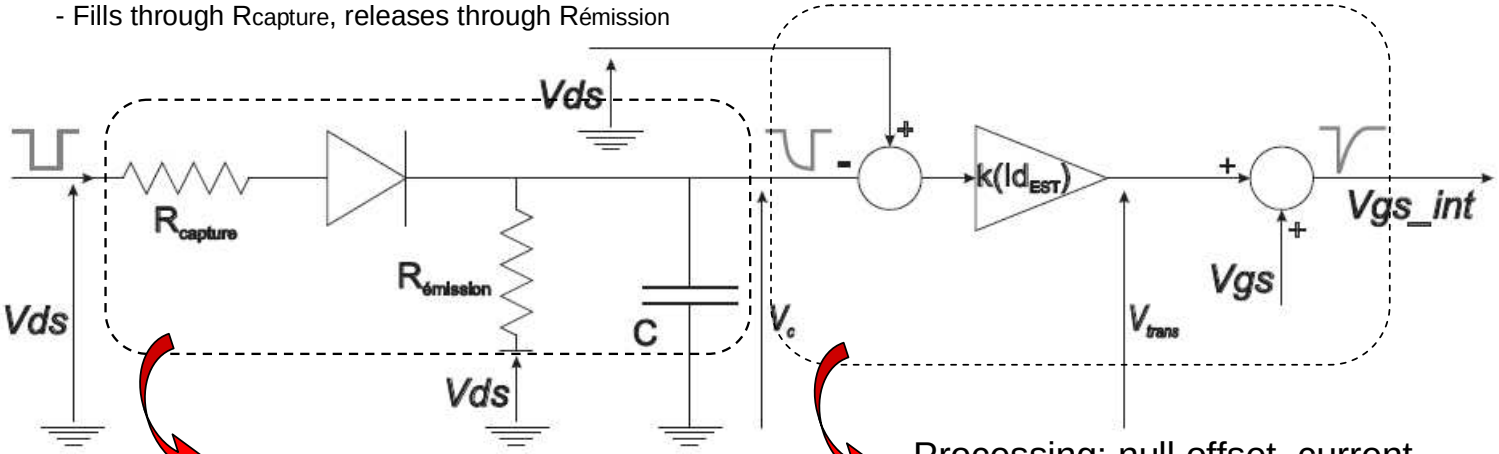
Vittorio Camarchia, *Member, IEEE*, Federica Cappelluti, *Member, IEEE*, Marco Pirola, *Member, IEEE*, Simona Donati Guerrieri, *Member, IEEE*, and Giovanni Ghione, *Fellow, IEEE*

Trapping effect Modelling

Gate- and drain-lag model topology (for ONE trap)

Trapping effect on the current modeled with a modification of the control voltage (= Vgs)

- Creates transients on Vgs = Current transients
- Charging state of the capacitance = charging state of the traps
- Fills through Rcapture, releases through Rémission



Fills and releases model of traps (diode)

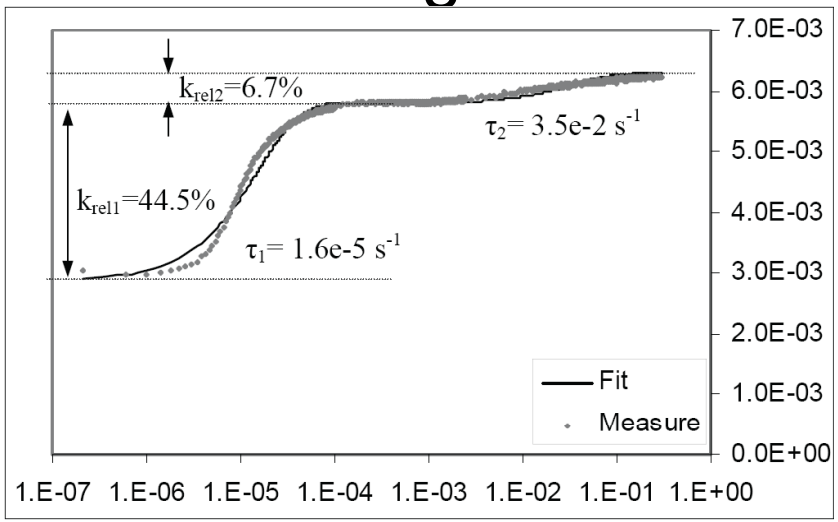
Processing: null offset, current dependencies, etc.
Easy tuning of the amplitude

Fundamental effect : fill / release trapping time constants are different
➔ modeled with an envelope detector

- Circuits number = Modeled traps number
- 3 parameters to extract per circuit : Rcaption, Rrelease, k

Trapping effect Modelling

Trap model parameters extraction



Current transient measurement, Negative pulse on Vds (emission)

➔Obtaining : - numbers of traps

- emission time constants

- relative amplitude of each trap

Avoid thermal effects during measurement

➔ **ONLY ONE MEASUREMENT TO OBTAIN ALL THOSE PARAMETERS**

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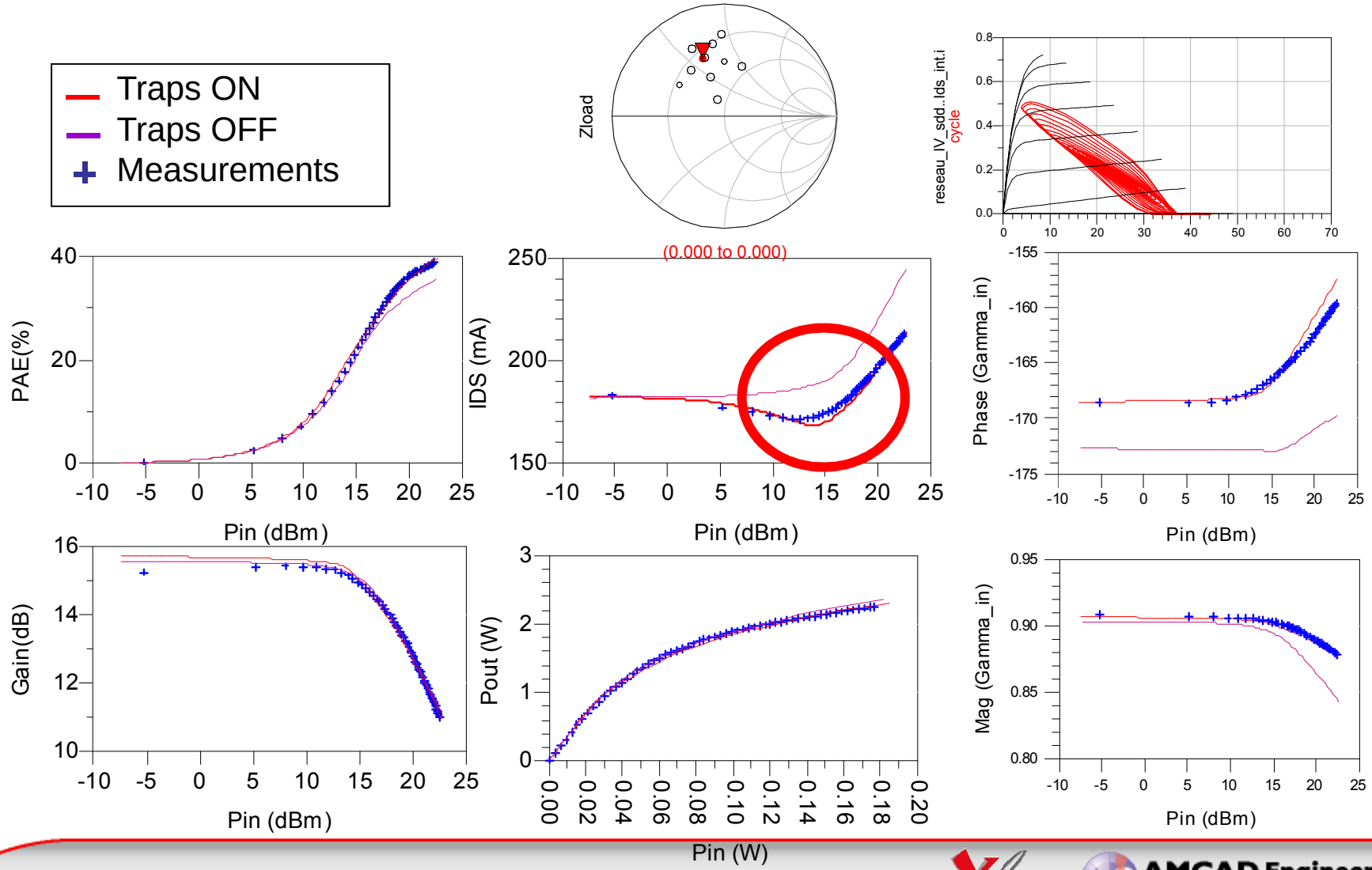
Model Validity : Large Signal

Measurements @ power optimal load impedance



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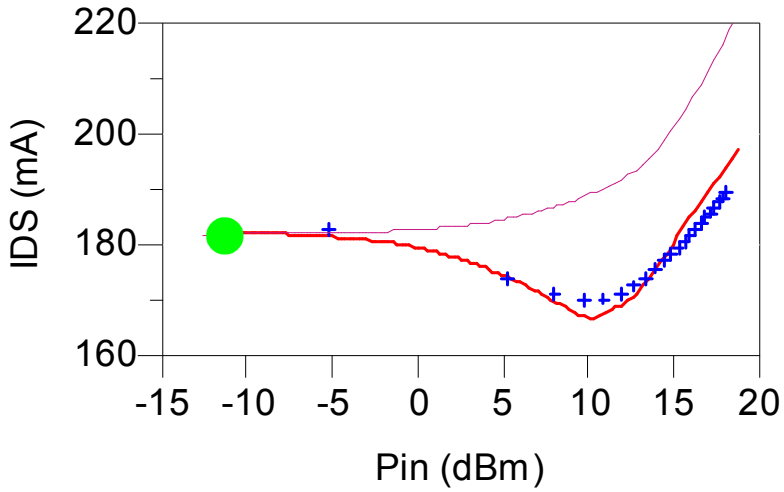
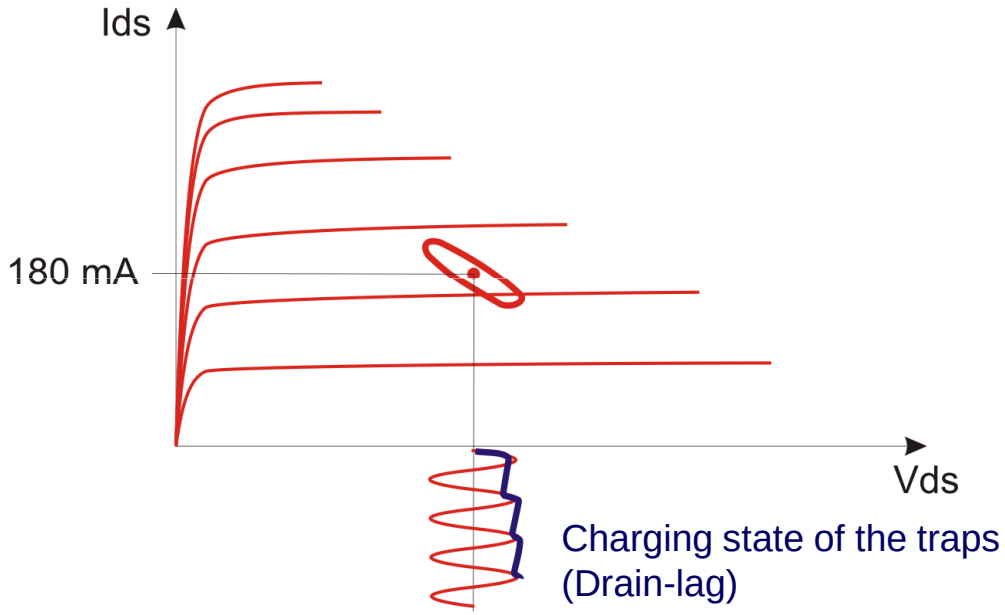
The current slope phenomenon





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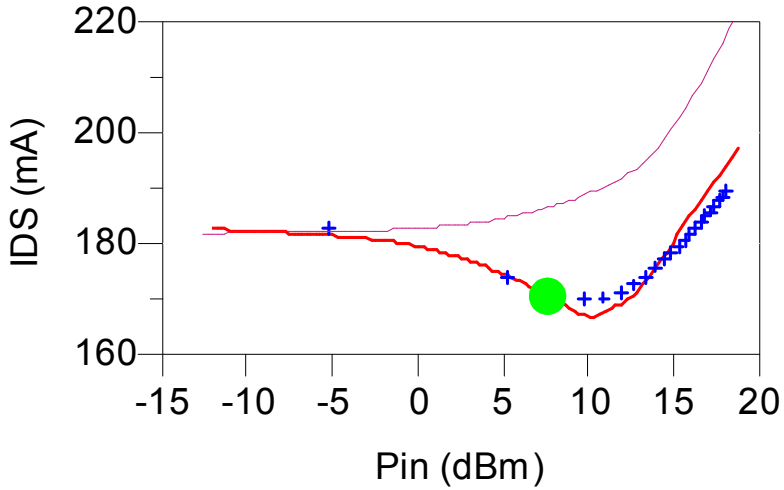
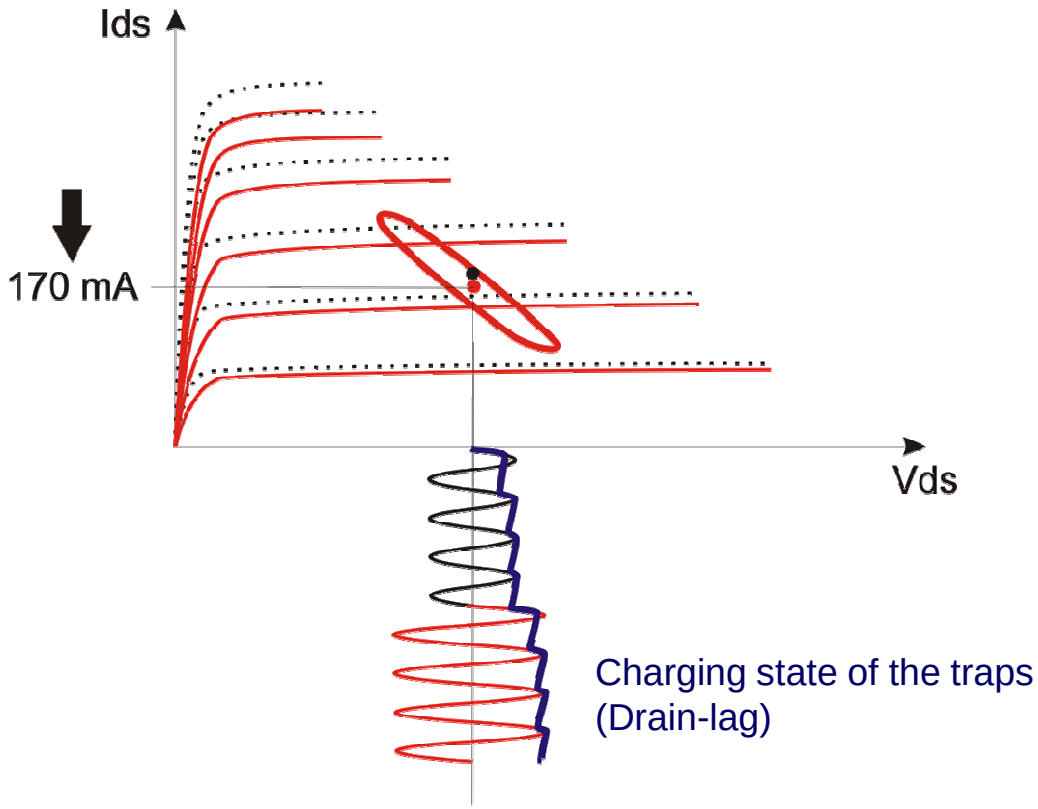
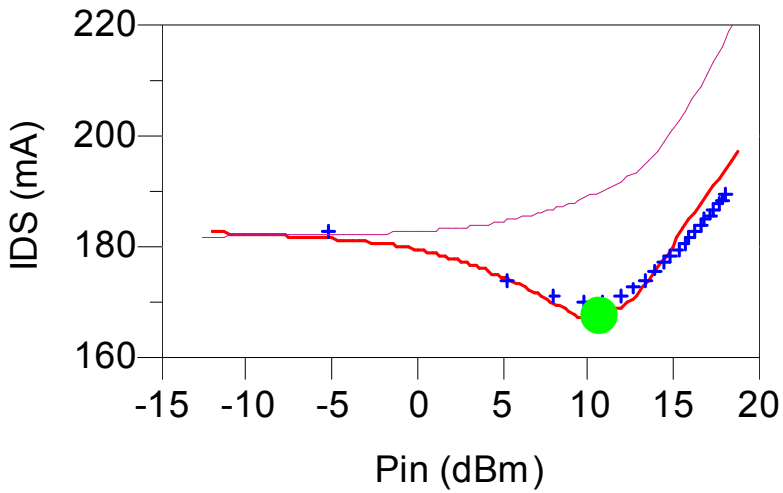
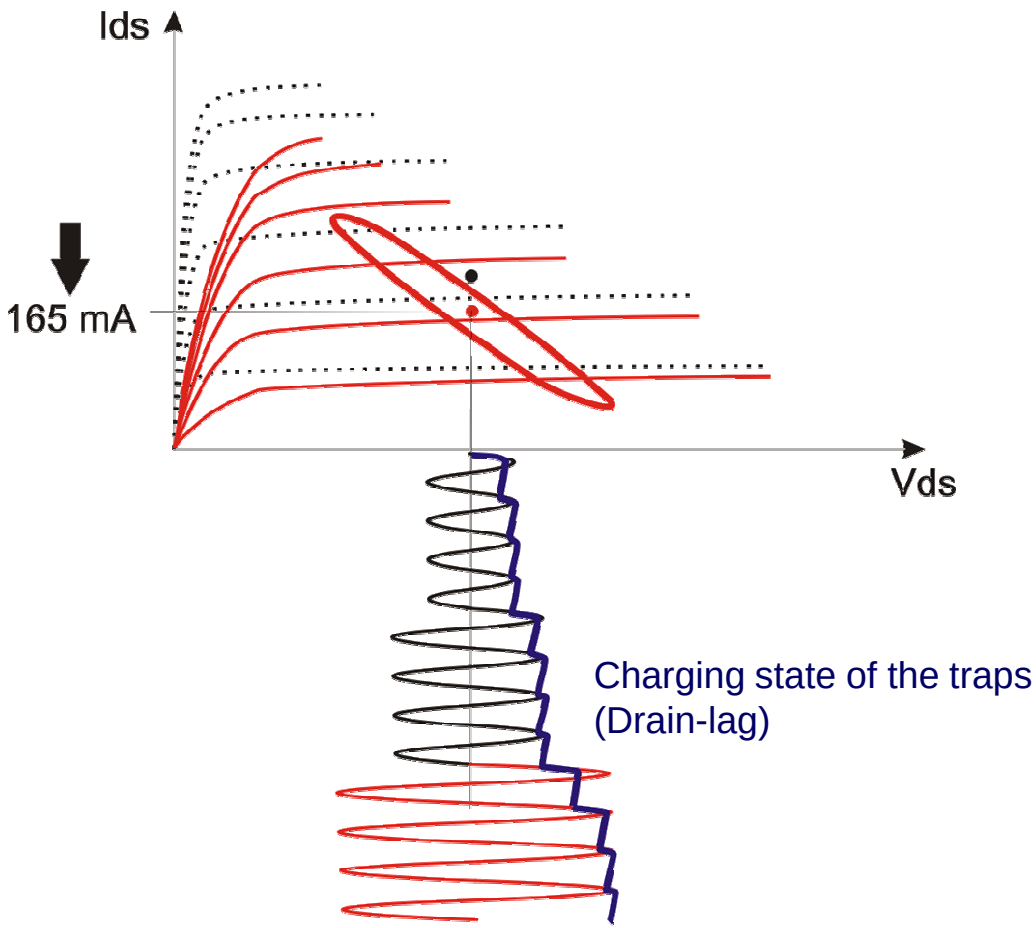




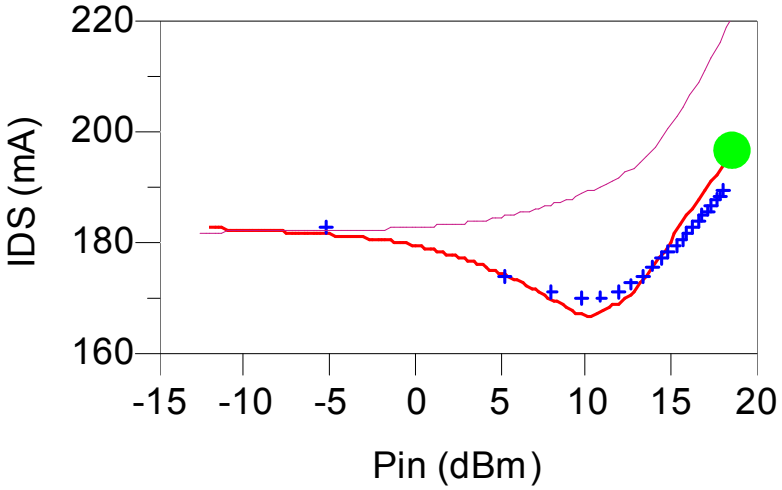
Charging state of the traps
(Drain-lag)

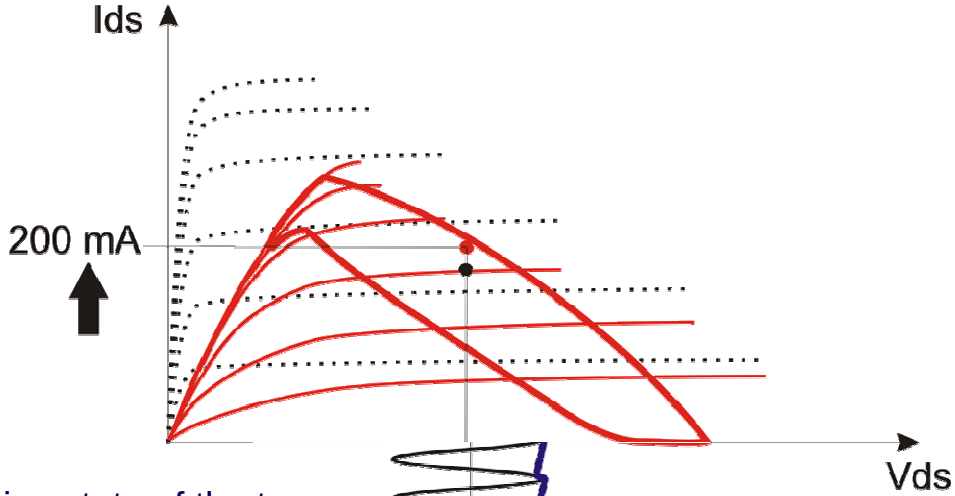
The current slope phenomenon





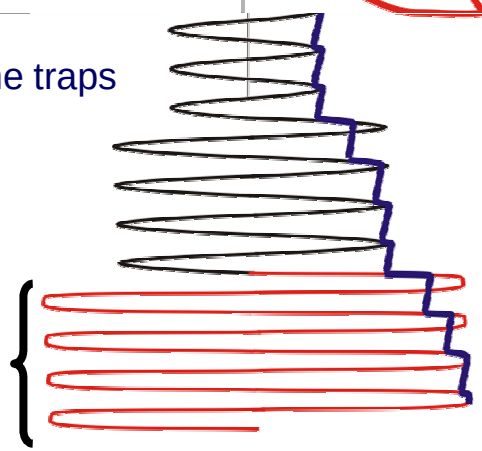
The current slope phenomenon





Charging state of the traps
(Drain-lag)

Saturation = Auto-bias



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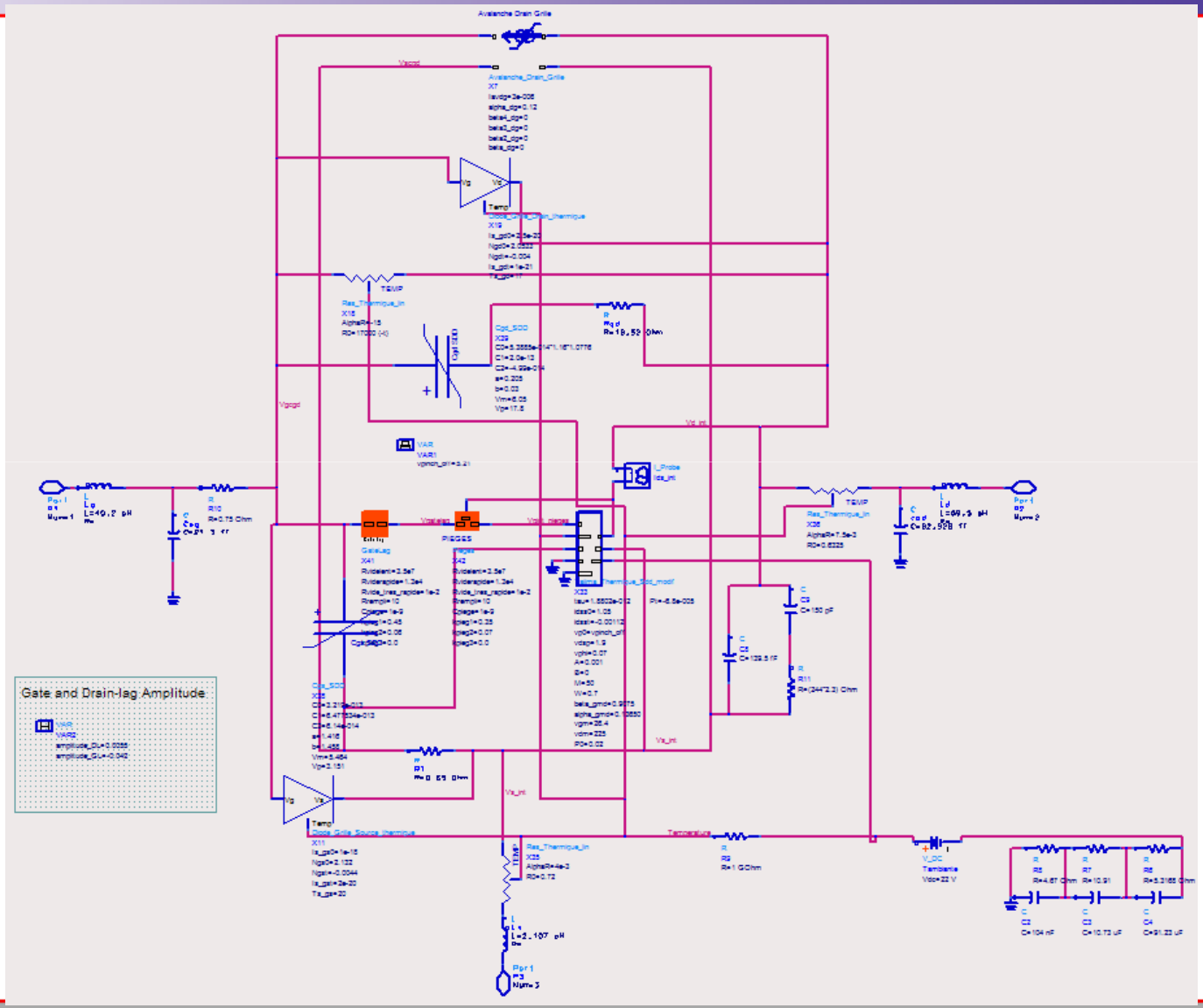
Completed Nonlinear Model



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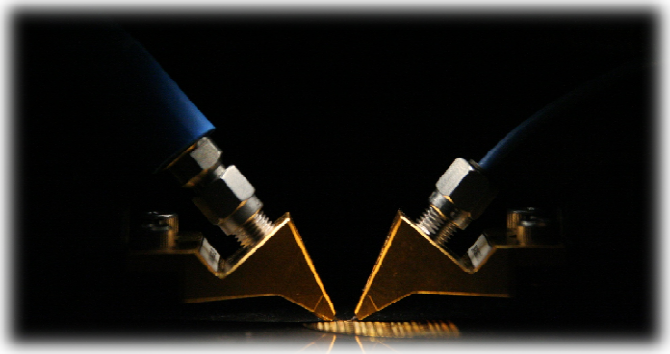
IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 55, NO. 12, DECEMBER 2007

An Electrothermal Model for AlGaN/GaN Power HEMTs Including Trapping Effects to Improve Large-Signal Simulation Results on High VSWR

Olivier Jardel, Fabien De Groote, Tibault Reveyrand, Jean-Claude Jacquet, Christophe Charbonniaud, Jean-Pierre Teyssier, Didier Floriot, and Raymond Quéré, *Senior Member, IEEE*

PART II : Load Pull Measurement setups

T. Gasseling (AMCAD Engineering)



Load Pull for PA Design : LPPD

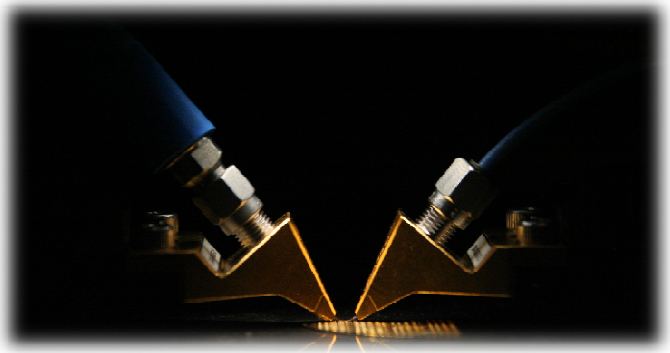
- The needs
- Existing architectures

Load Pull for Model Validation : LPMV

- Specific needs
- Measurement definition
- Specific Architecture

News trends

- Time domain measurements for model validation



Load Pull used for PA Design : LPPD

- The needs
- Existing architectures

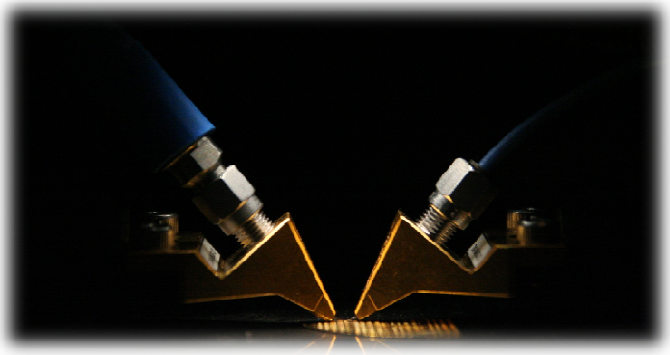
Load Pull used for model validation : LPMV

- Specific needs
- Measurement definition
- Specific Architecture

News trends

- Time domain measurements for model validation

Load Pull for PA Design



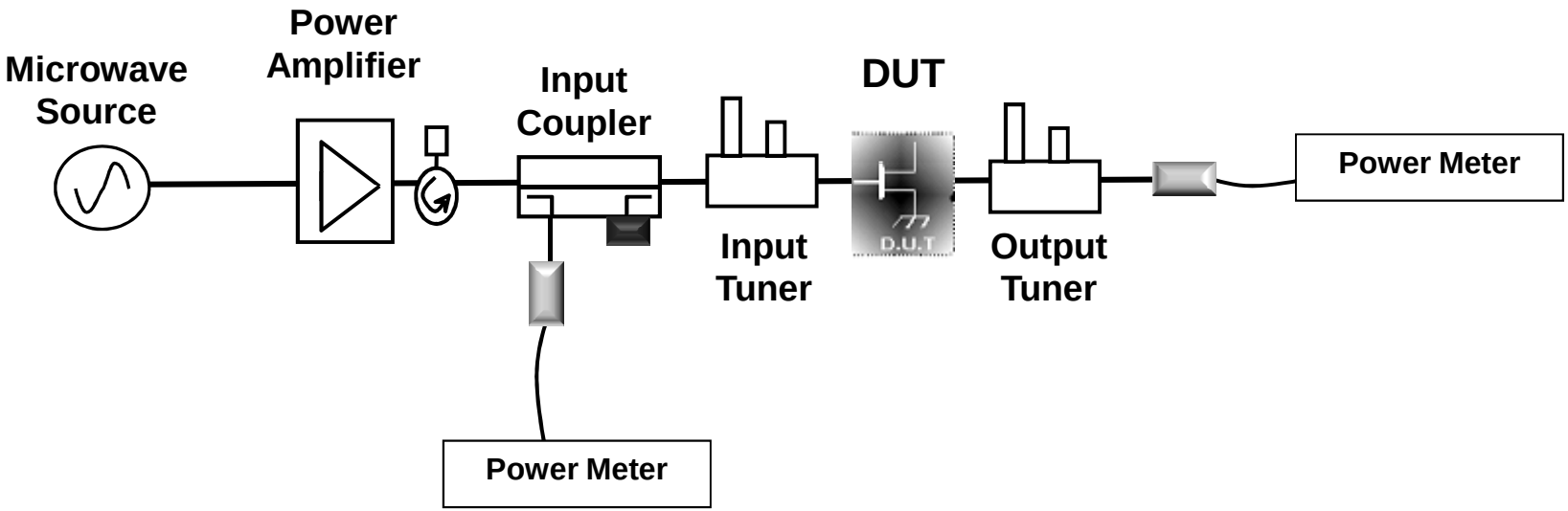
The needs:

From the target definition (Pout, Efficiency, Gain ect.)

- **Power performances versus Zsource and Z load**
- **ISO-circles plot -> Determination of optimal operating conditions**
- **Transistor performances evaluation associated to given operating conditions for the design of PA.**
- **Transistor model validation**

Load Pull for PA Design

LPPD architecture



The LPPD setups have been developed in order to find the transistor's optimal source and load impedances for defined and fixed operating conditions

These LPPDs setups can be used for:

Transistor performances evaluation for given operating conditions (transistor + setup combination)

Determination of optimal load impedances : useful for PA design when nonlinear models are not available

These LPPDs setups can not be used for:

A determination of the intrinsic transistor characteristics useful for transistor model validation.

Can a LPPD setup measure Power Added Efficiency?

The answer is: NO. A passive load pull system measures the **source power (available)** toward the input of the DUT and the **power delivered by the DUT to the load**.

If a directional coupler is used to measure the power returned by the DUT to the source, in order to assess the really absorbed power by the DUT, then the loss of the input tuner and the coupler **can only be calculated if we know the large signal input impedance of the DUT**.

However*:* If the **DUT is perfectly input matched** and **only then**, the Efficiency measured equals the Power Added Efficiency defined as:

PAE = (Power delivered to load – Power delivered to DUT) / (DC power);
and the Gain measured becomes Power Gain

Gp = Pout-del / Pin-del

But one has to be careful: If the DUT is tuned at the input so that the reflected power to the source (measured via the 4rth port of the input coupler or the third port of a circulator) becomes zero, **this does not mean** the DUT is "input matched", **it means that the setup is matched at the intersection between tuner and circulator, not tuner and DUT**

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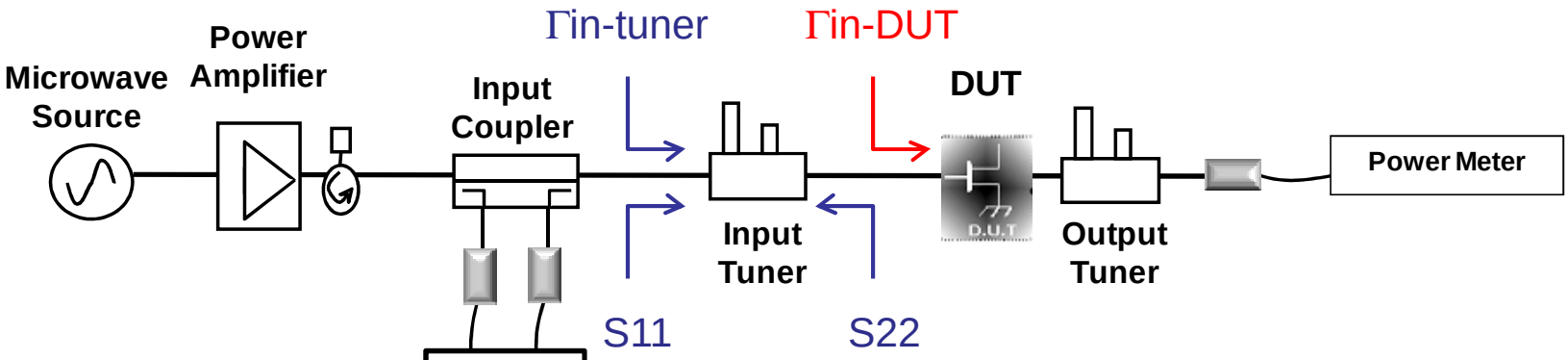
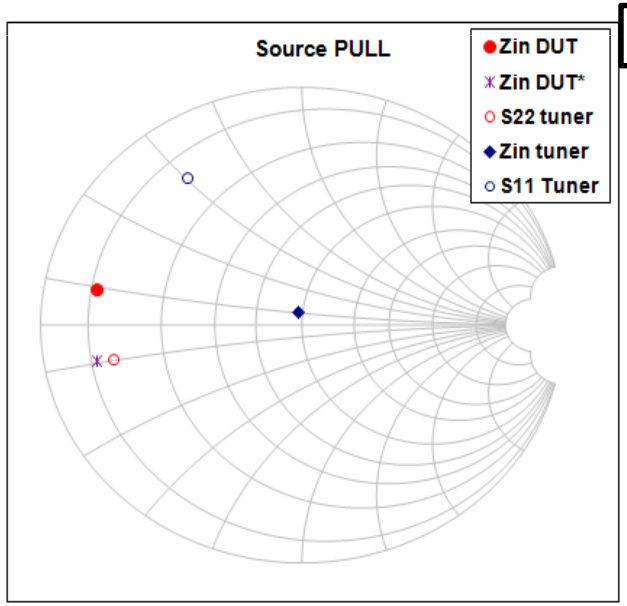
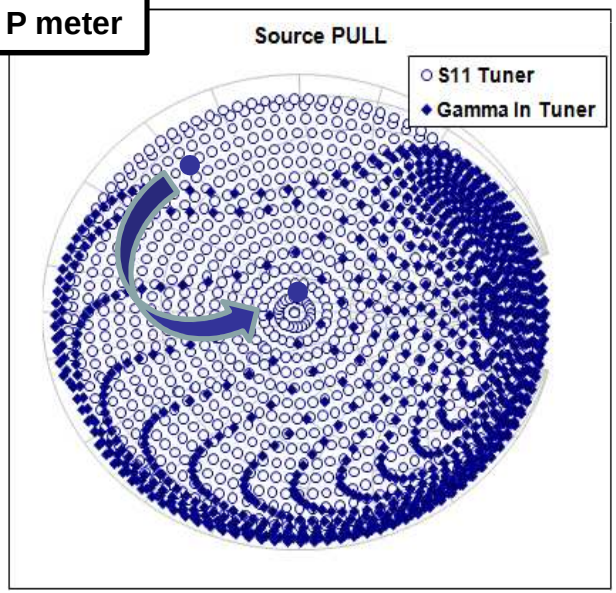
Illustration : Measurements on a FET @ f0=4GHz







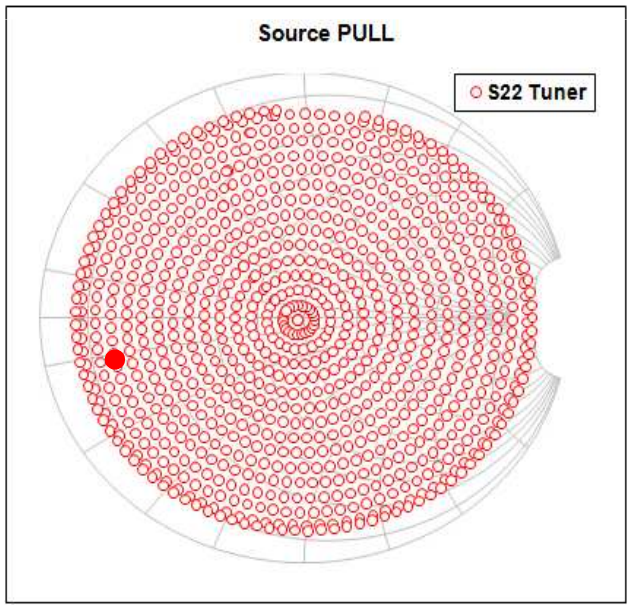


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Illustration : Measurements on a FET @ f0=4GHz

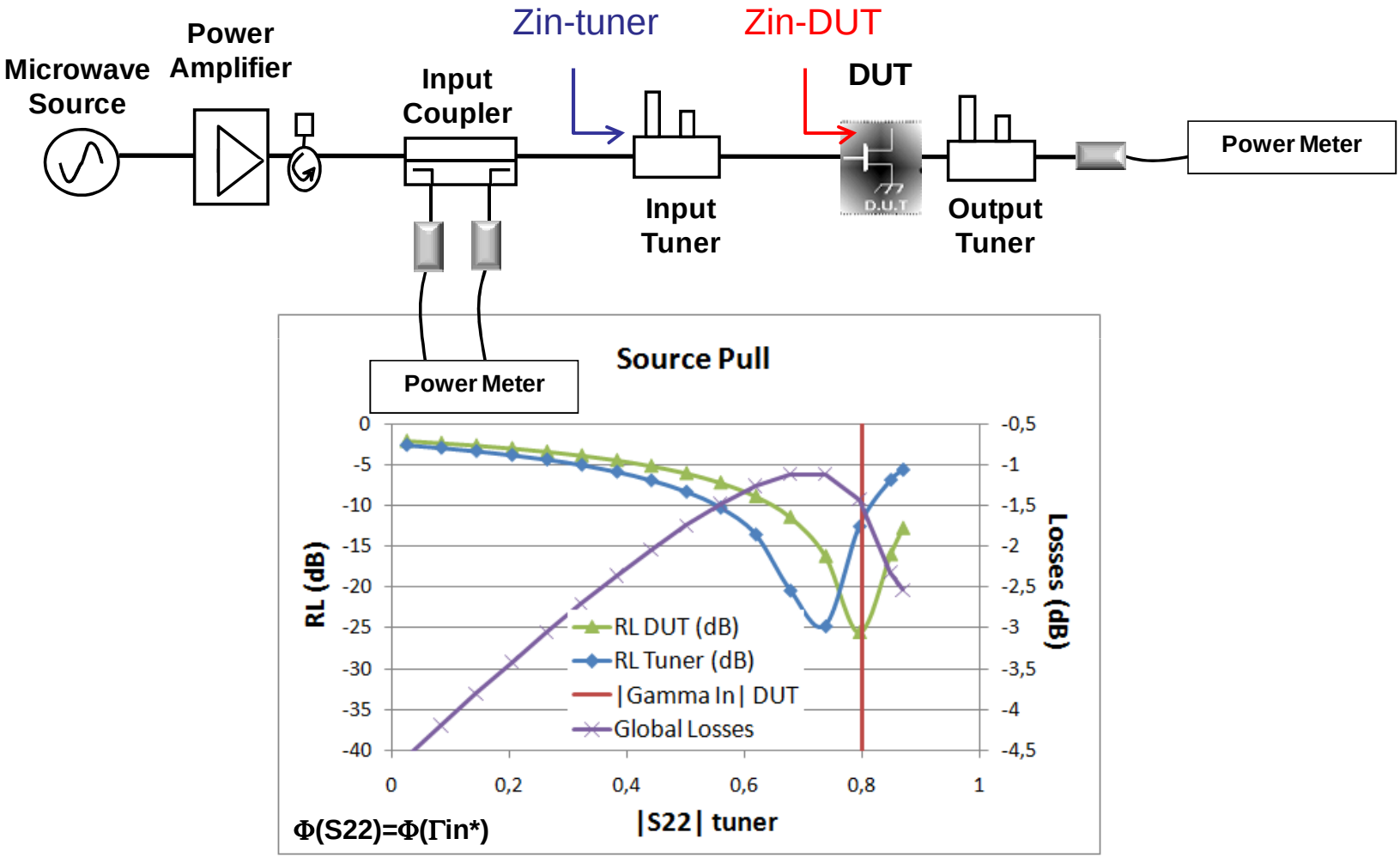

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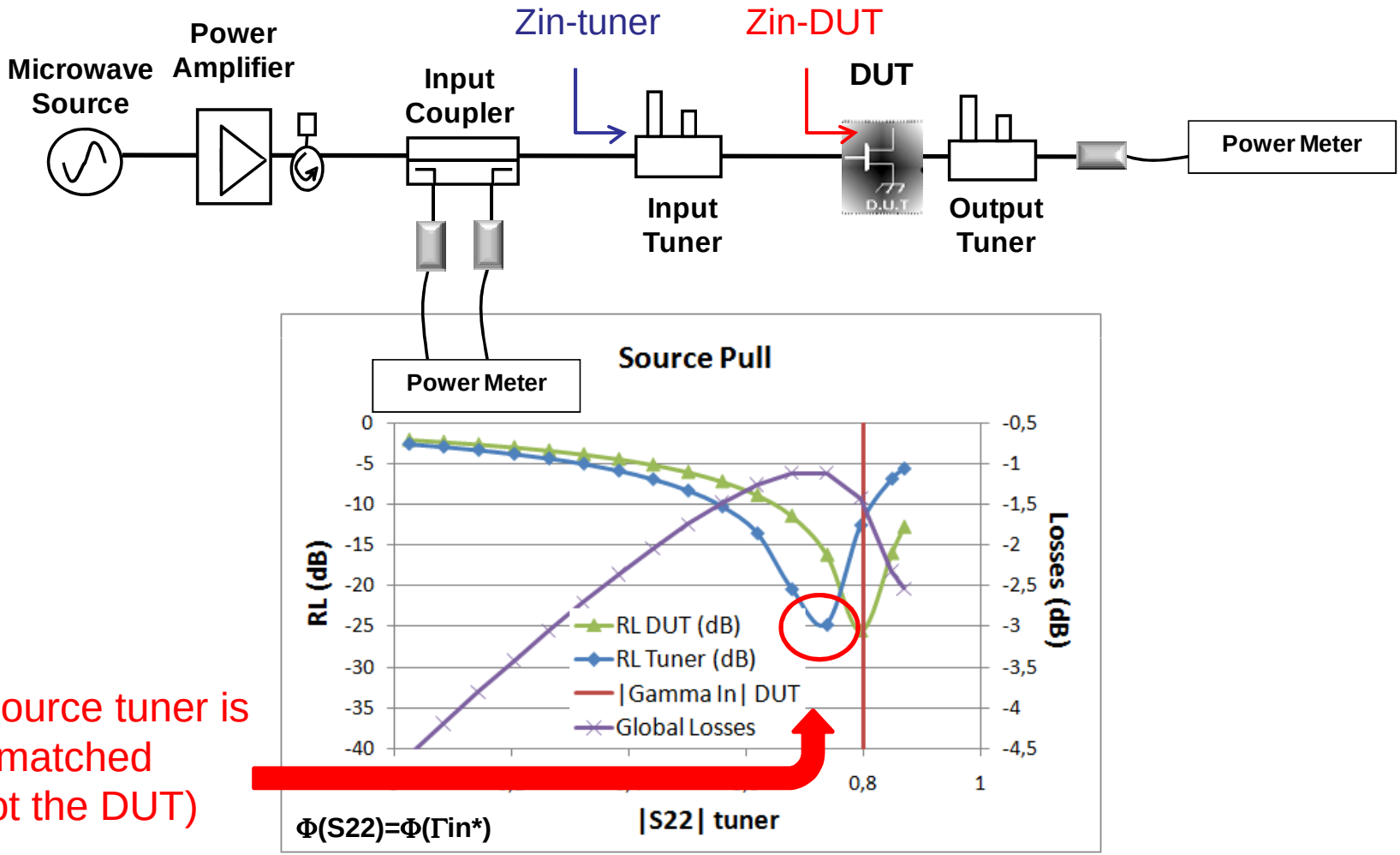
Illustration : Measurements on a FET @ f0=4GHz



The source tuner is matched (not the DUT)

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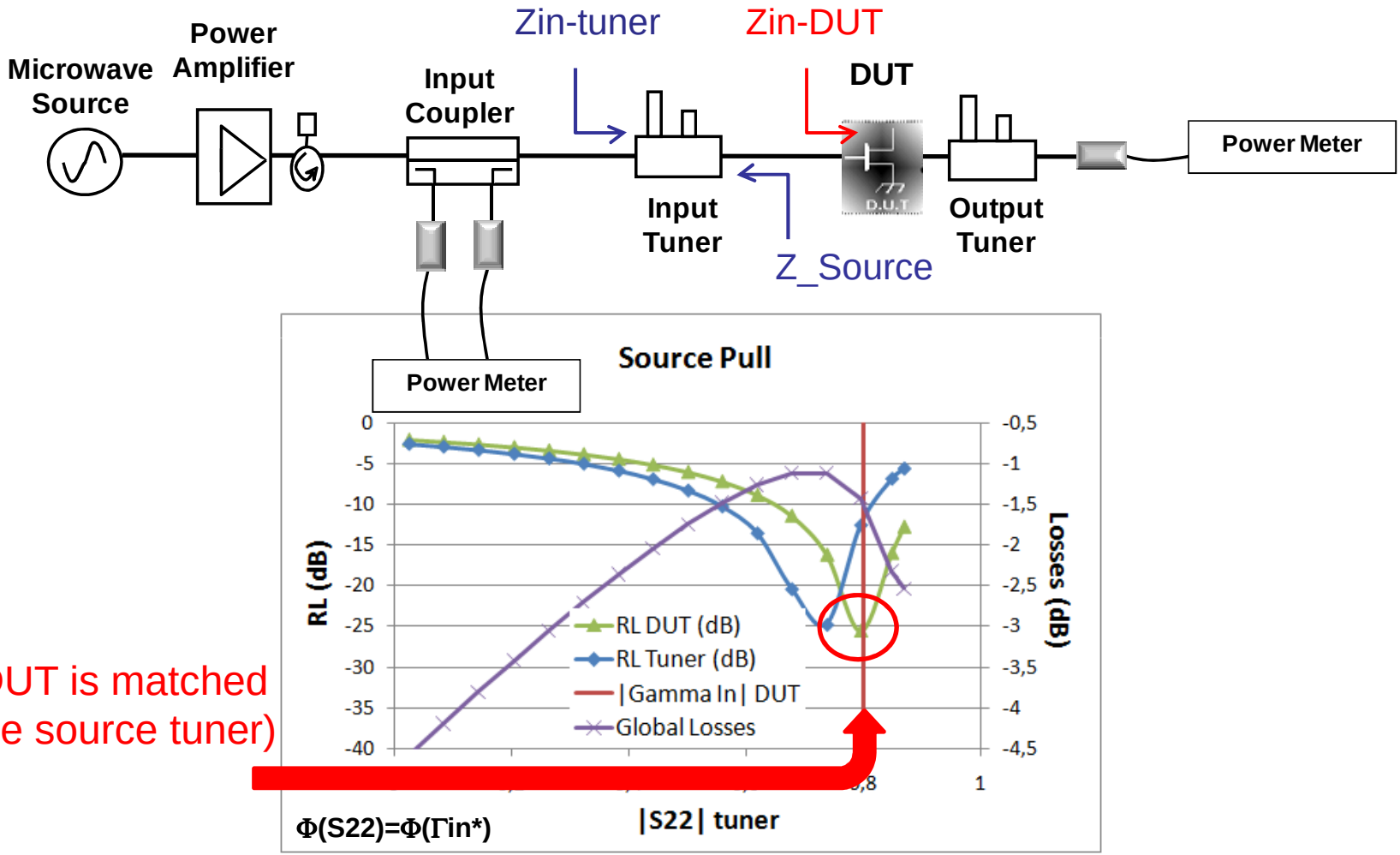
Illustration : Measurements on a FET @ f0=4GHz



The DUT is matched
(not the source tuner)

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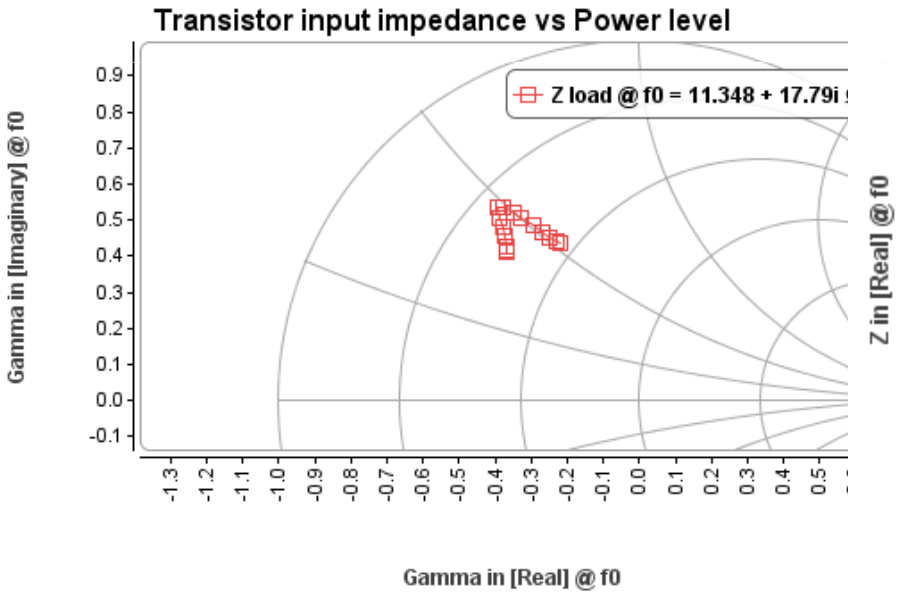
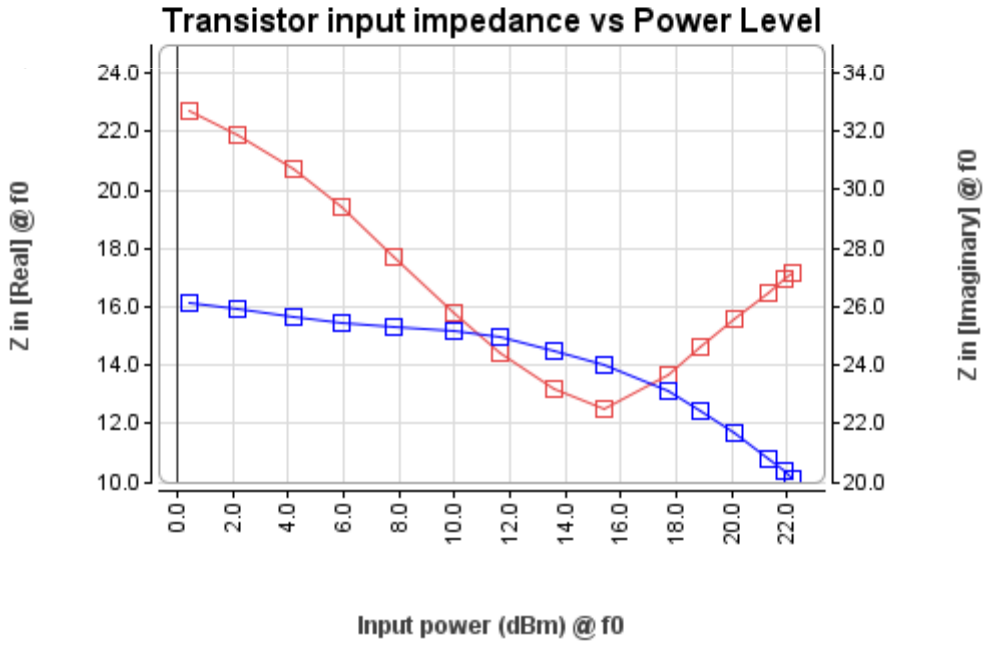
Can a PA Load Pull System measure Power Added Efficiency? : **The answer is: NO**.

The assumption that the Efficiency measured equals the Power Added Efficiency only when the "**DUT is input matched"** and **only then**, means that this assumption is valid only when the source pull optimization (iso-Pout or Gain circles) is done for a **constant** amount of input power injected into the DUT.

As a consequence, because the transistor's input impedance is related to the amount of power injected in the DUT, this optimization must be done for each power level.





Conclusion :

Each time the power injected in the DUT is varied, the transistor input impedance is varied as well, and then the assumption of the perfect matching at the input could not be done any more.

If the transistor's intrinsic PAE needs to be measured, then the source impedance should be optimized for each power step : cumbersome and time consuming

Ordinary load pull architecture are useful for PA designers but raw data such as gain and Efficiency measurements **are not accurate enough to be used for model validation**.

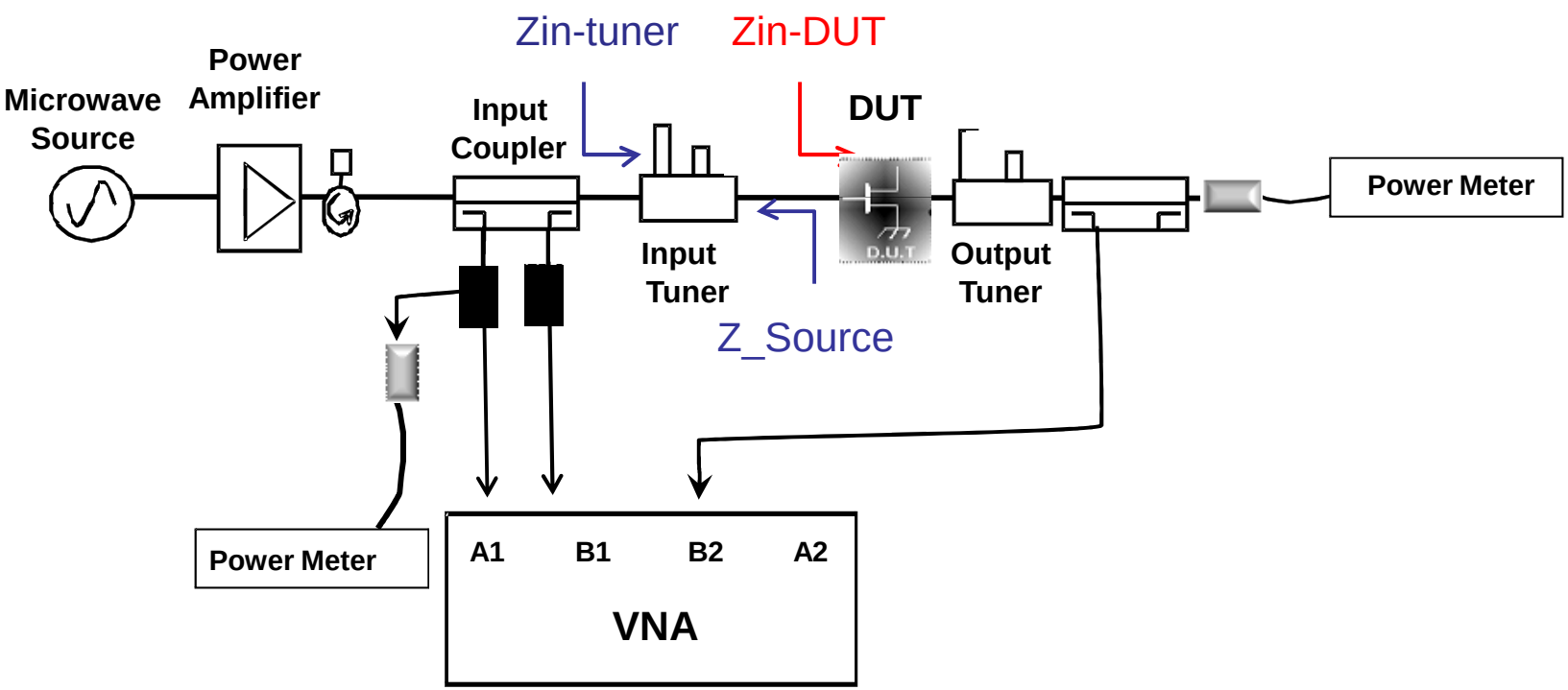
Conclusion :

In addition, measurements made with power meters are mean power measurements.

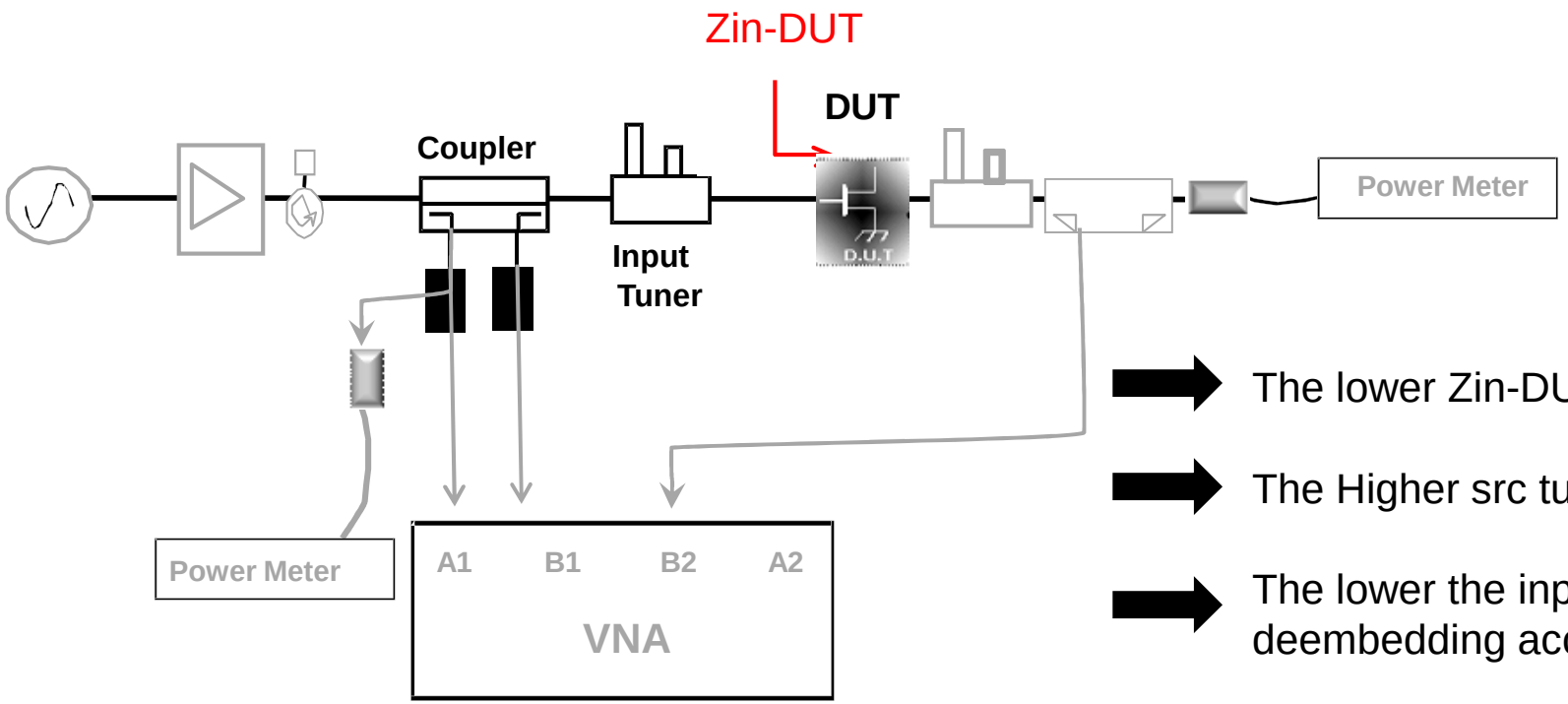
When in the bandwidth of the power sensor, the power measured corresponds to the power generated at the fundamental and harmonic frequencies,.

For model validation, the wanted power (at the fundamental frequency) and the power generated at harmonic frequencies, should be measured independently.

Some LPPDs setups have been updated in order to measure the transistor's input reflection coefficient:



Some LPPDs setups have been updated in order to measure the transistor's input reflection coefficient:



- The lower Zin-DUT
- The Higher src tuner losses
- The lower the input deembedding accuracy
- Problem : The transistor power gain is really sensitive to the Γin meas accuracy.

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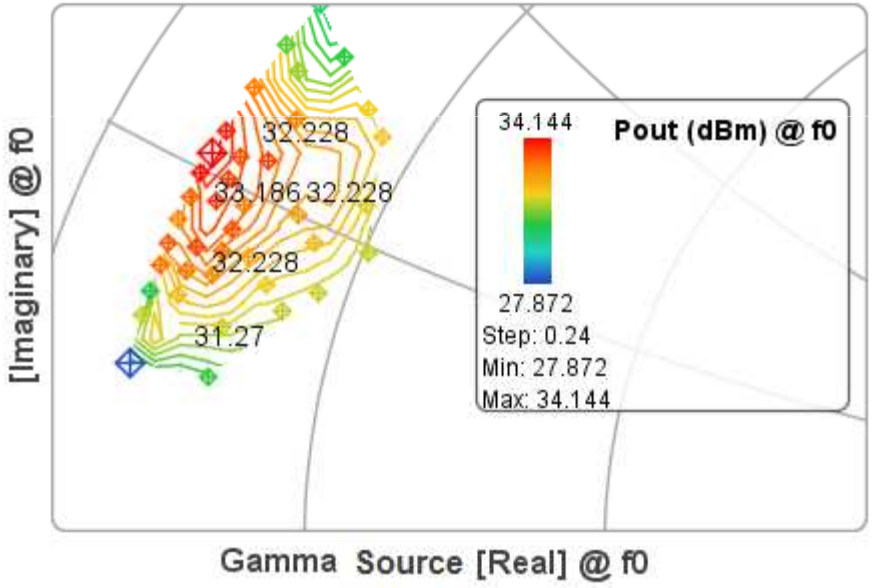
Illustration : Gin measurements / LPPD setups

Source pull : for each source impedance, the Gin measurement is de-embedded through a new input tuner's set of S2P bloc file.

While the measurement accuracy if data such as Pout or Transducer Power gain versus Zsource are convenient for PA design ..



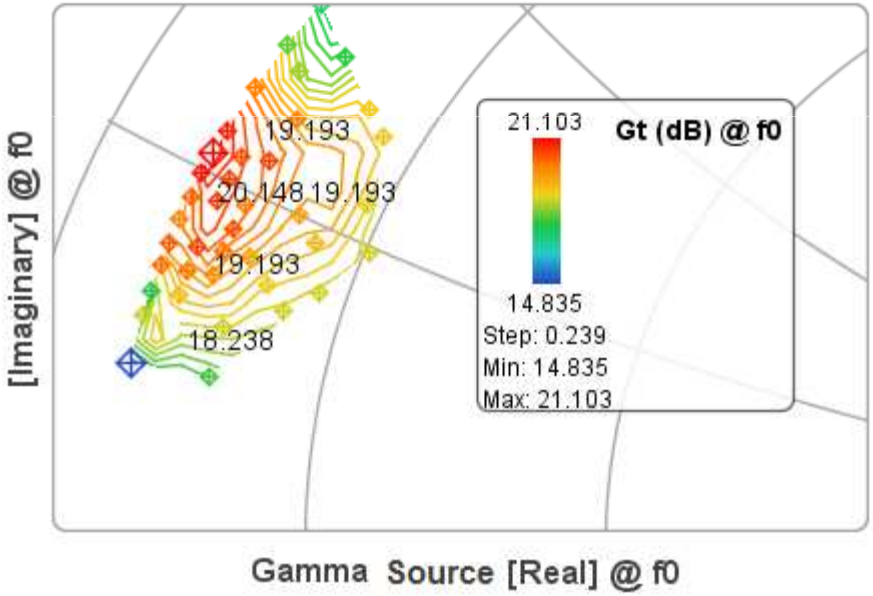


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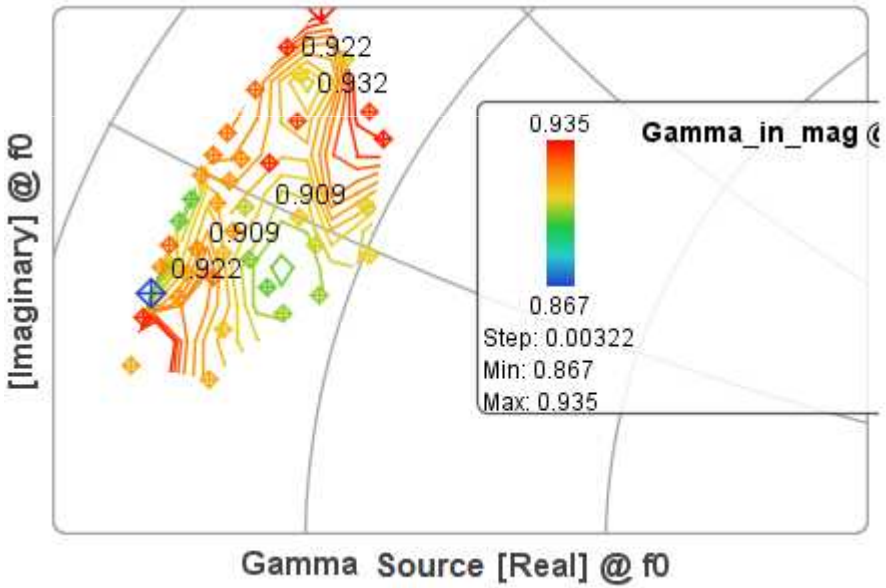
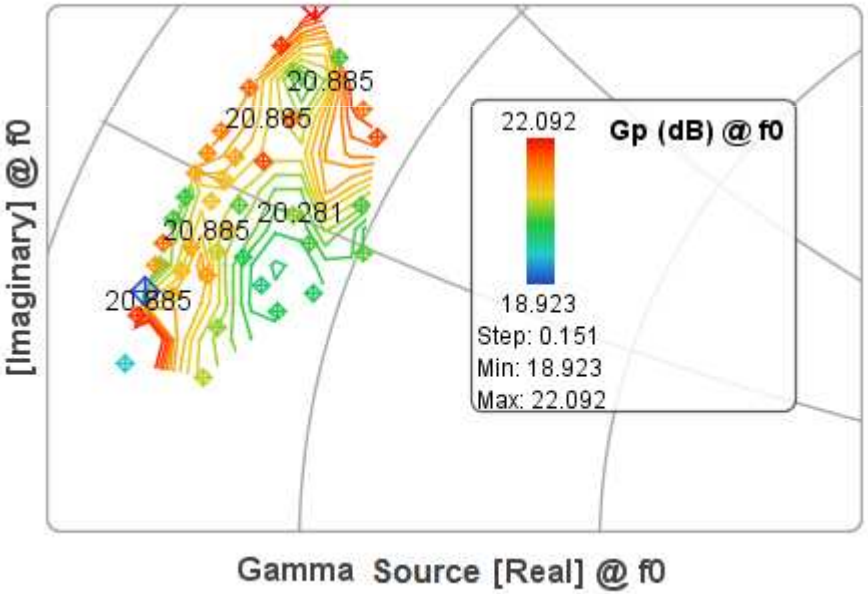
Illustration : Gin measurements / LPPD setups

Source pull : for each source impedance, the Gin measurement is de-embedded through a new input tuner's set of S2P bloc file.

Some of them such as |Γin| or power gain are not accurate enough for Model validation





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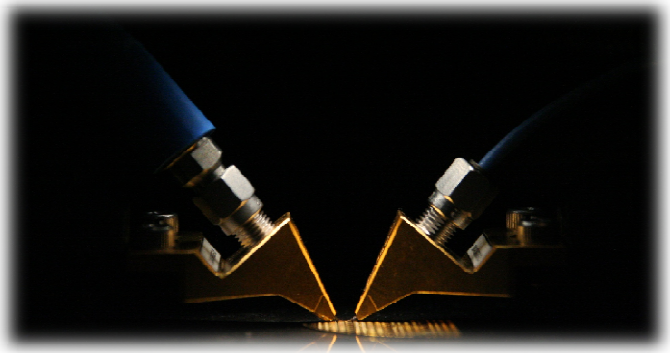


Load Pull used for PA Design : LPPD

The needs

Existing architectures

Load Pull used for Model Validation : LPMV

Specific needs

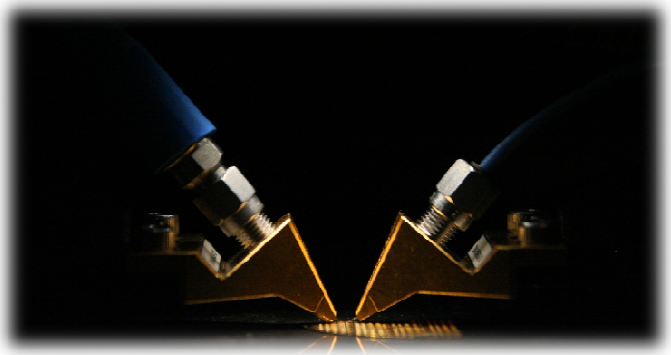
Measurement definition

Specific Architecture

News trends

Time domain measurements for model validation

Load Pull used for Model Validation

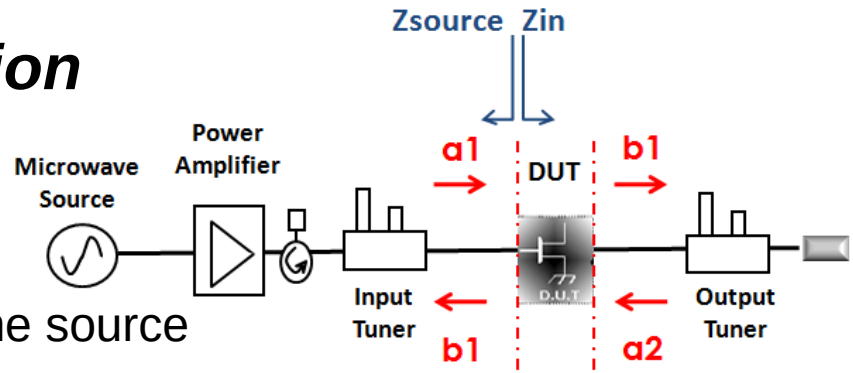


Specific needs

- Measurement of the transistor input impedance, whatever the operating conditions (Zload, Power level ect.)
- Narrow band measurements at f0, 2f0, 3f0 ect.
- True calculus of Γin, PAE, Gain ...
- Transistor model validation

Load Pull used for model validation

Measurement definition



P_in: Power delivered to the DUT by the source

$$P_{in} = \frac{1}{2}\left(|a1|^2 - |b1|^2\right) = \frac{1}{2}|a1|^2 * \left(1 - |\Gamma in|^2\right)$$

P_source: Power delivered by the source

$$P_{source} = \frac{P_{in}}{1 - \left|\frac{Zin - Zsource^*}{Zin + Zsource}\right|^2}$$

P_out: Power delivered to the load impedance

$$P_{out} = \frac{1}{2}\left(|b2|^2 - |a2|^2\right) = \frac{1}{2}|b2|^2 * \left(1 - |\Gamma load|^2\right)$$

Load Pull used for model validation

Measurement definition

Used for model validation

Power gain is the ratio of the power delivered to the load (**P_{out}**) to the power delivered to the transistor by the source (**P_{in}**).

$$Gain_{power} = \frac{Pout}{Pin} = \frac{|b2|^2(1-|\Gamma load|^2)}{|a1|^2(1-|\Gamma in|^2)}$$

Used for PA design

Transducer Power gain is the ratio of the power delivered to the load (Pout) to the power available from the source (Psource).

$$Gain_{trans} = \frac{Pout}{Psource} = \frac{|b2|^2(1-|\Gamma load|^2)}{|a1|^2(1-|\Gamma in|^2)} * \left(1 - \left|\frac{Zin - Zsource*}{Zin + Zsource}\right|^2\right)$$

$$Gain_{power} = Gain_{trans} \quad if \;\; Zin = Zsource*$$

Load Pull used for model validation

Measurement definition

Used for model validation

Power added Efficiency is the ratio of the power added by the transistor to the power consumed.

$$PAE = \frac{(Pout - Pin)}{PDC}\%$$

Used for PA design

Transducer Efficiency is the ratio of the power added by the source + transistor to the power consumed.

$$Eff = \frac{(Pout - Psource)}{PDC}\%$$

$$PAE = Eff \quad if \;\; Zin = Zsource*$$

Load Pull used for model validation

Measurement definition

Used for model validation

Power added Efficiency is the ratio of the power added by the transistor to the power consumed.

$$PAE = \frac{(Pout - Pin)}{PDC}\%$$

Used for PA design

Transducer Efficiency is the ratio of the power added by the source + transistor to the power consumed.

$$Eff = \frac{(Pout - Psource)}{PDC}\%$$

$$PAE = Eff \quad if \;\; Zin = Zsource*$$

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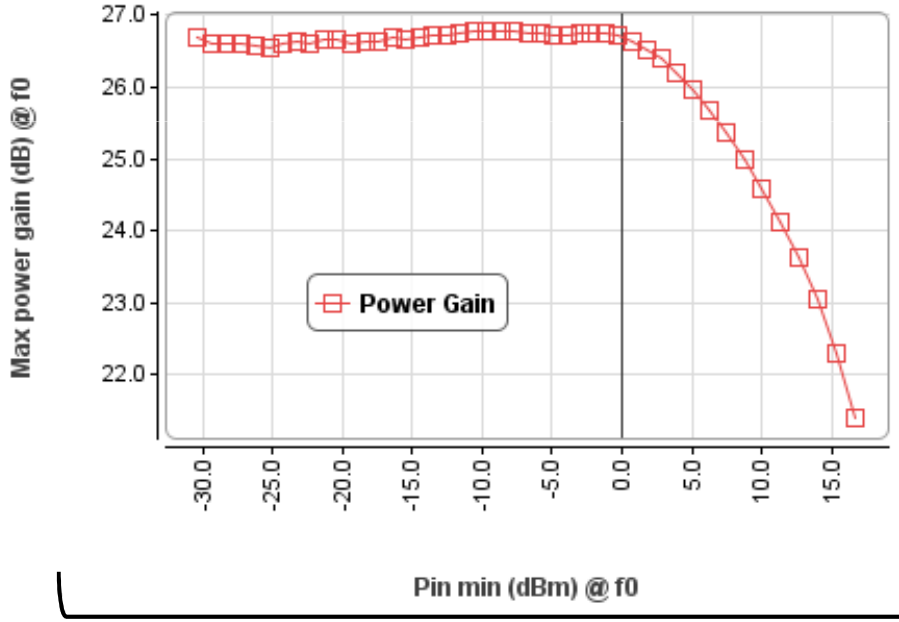
Illustration : Measurements on a FET @ f0=4GHz

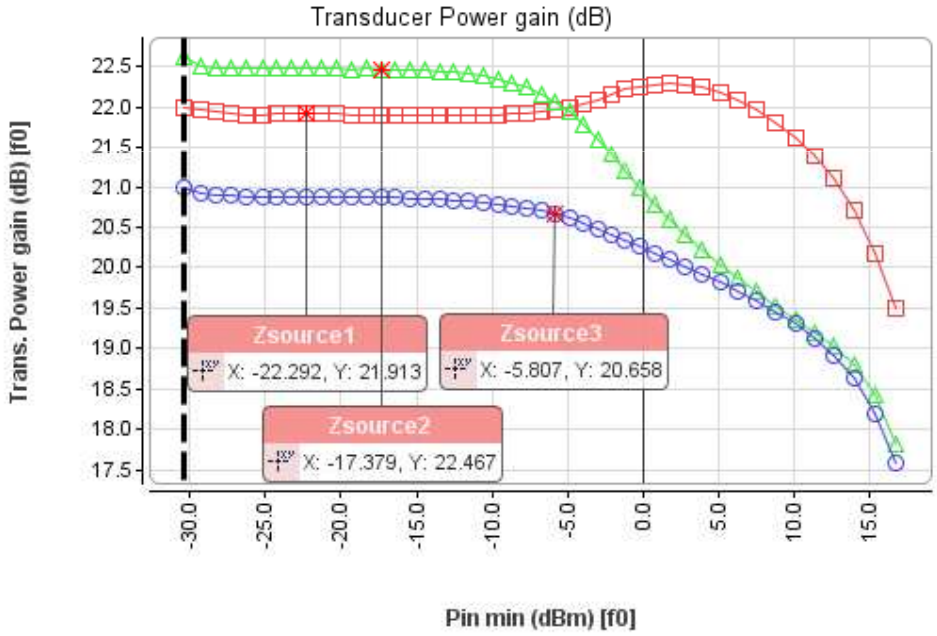
Used for model validation

Power gain



Used for PA design

Transducer Power gain



Measurements done on the same transistor

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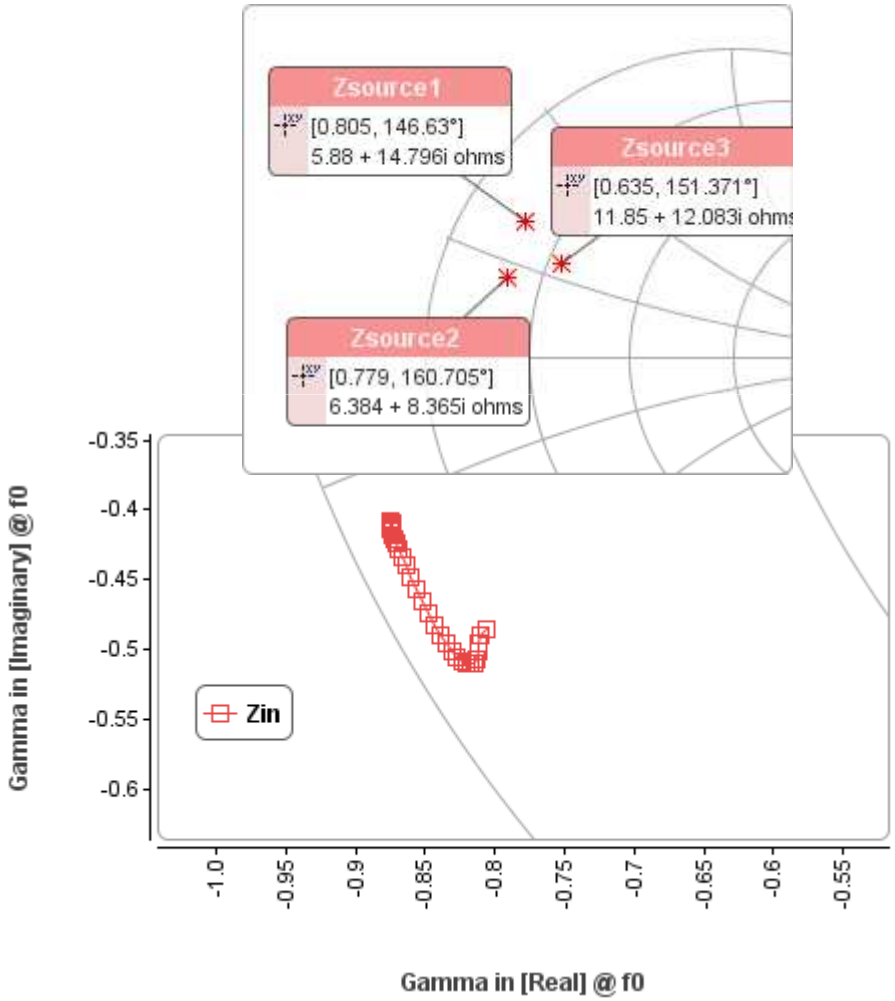
Illustration : Measurements on a FET @ f0=4GHz



Used for PA design

Transducer Power gain

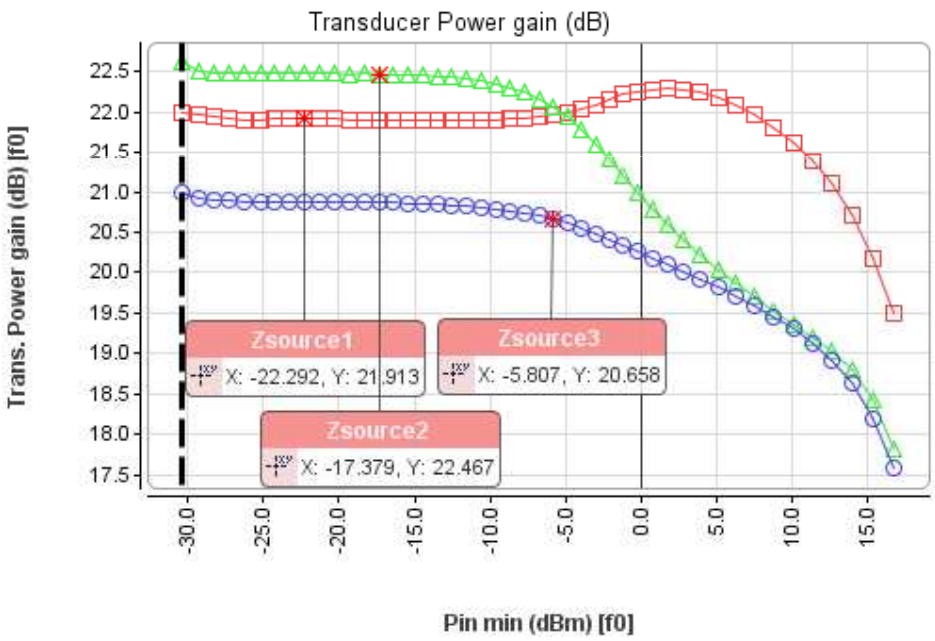


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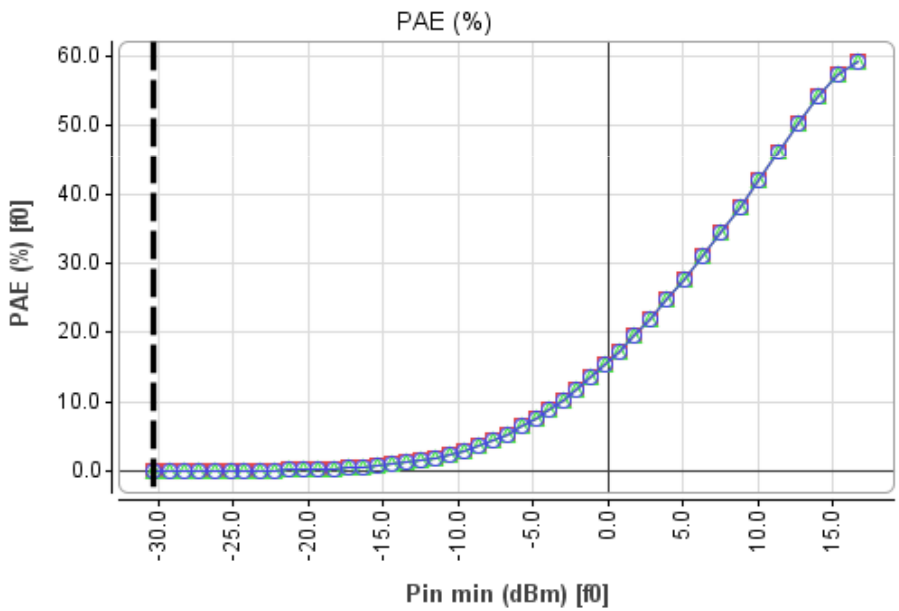
Illustration : Measurements on a FET @ f0=4GHz

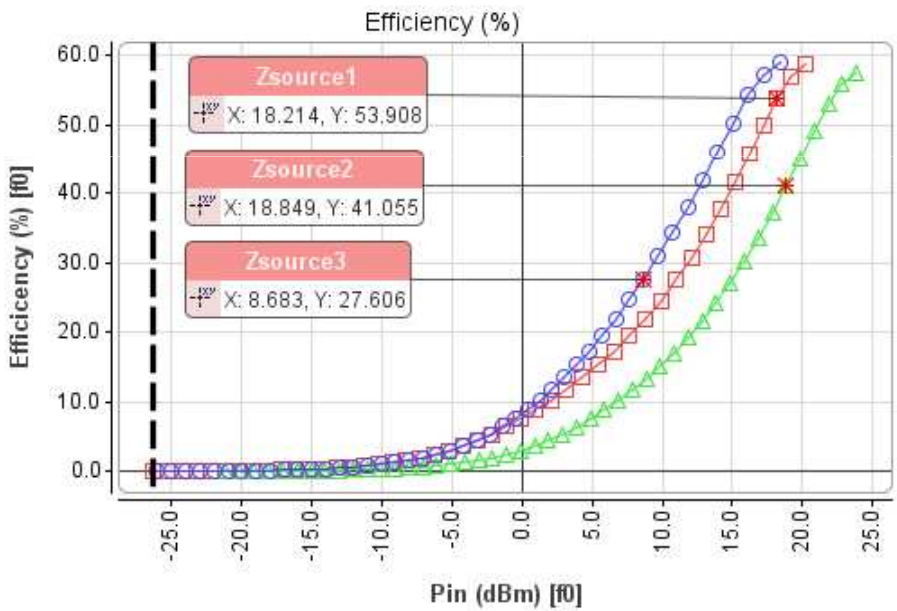
Used for model validation

PAE



Used for PA design

Transducer Efficiency



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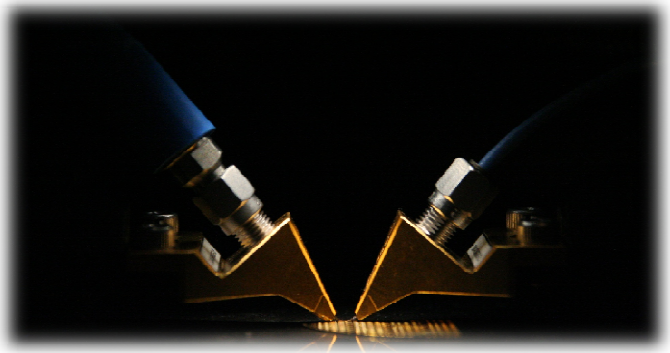
Load Pull used for model validation



Specific Architecture

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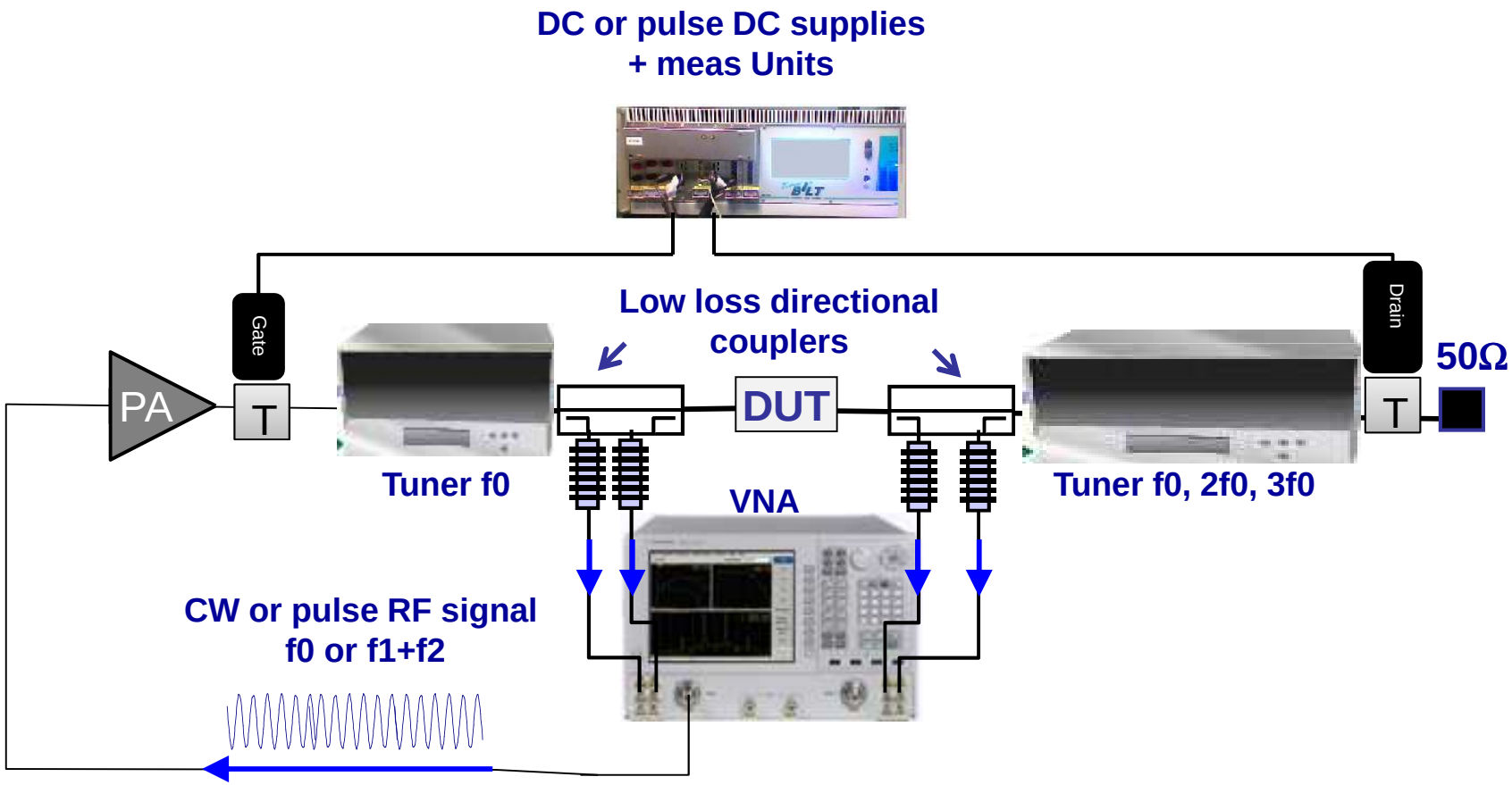
Specific Architecture



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Specific Architecture

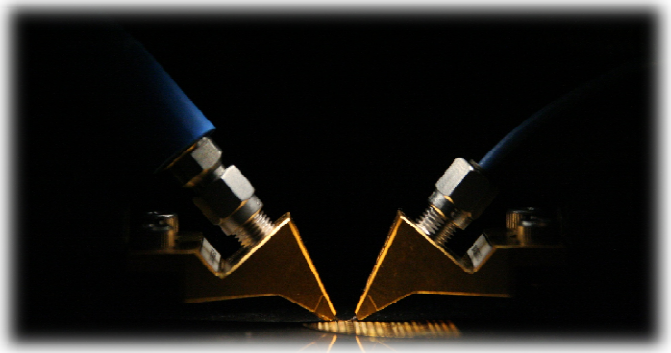
AMCAD Load Pull system used for modellng activities

AMCAD Engineering
Advanced Modeling for Computer-Aided Design

Conclusion

Model validation using load pull measurements : VNA use instead of power meters

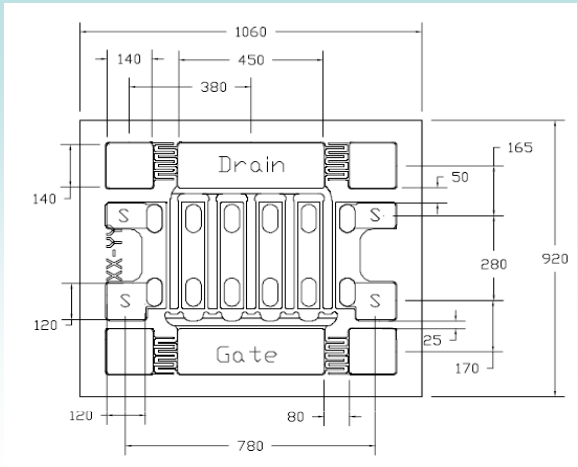
- ***Measurement in narrow band mode = F0 meas. + 2F0 meas. Instead of mean power meas.***
- ***Better dynamic range = better meas. Accuracy***
- ***Vector measurement s instead of scalar measurements = useful data for model validation***

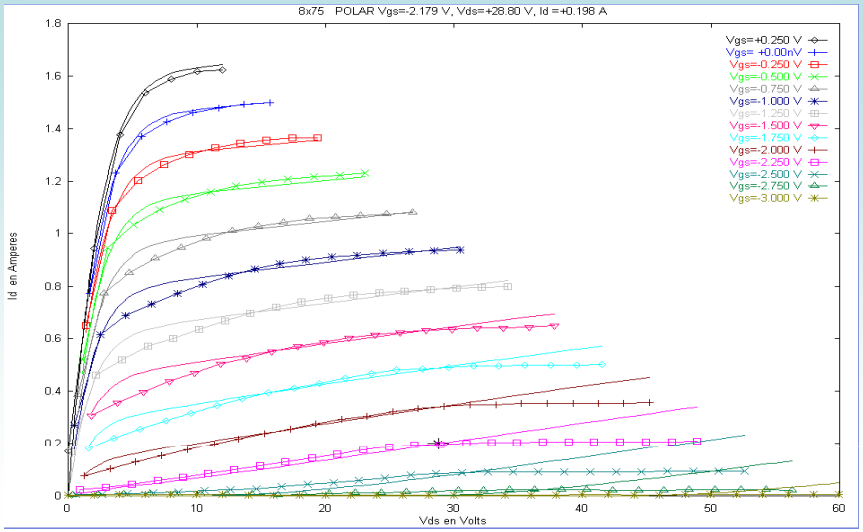


News trends

Time domain measurements for model validation

Time domain measurements for MMIC validation





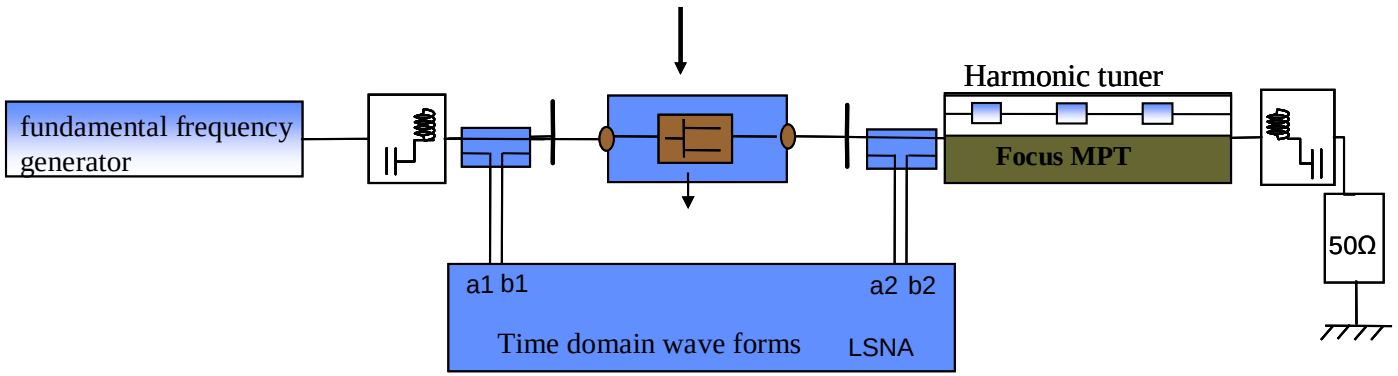
Characteristics of transistor used:

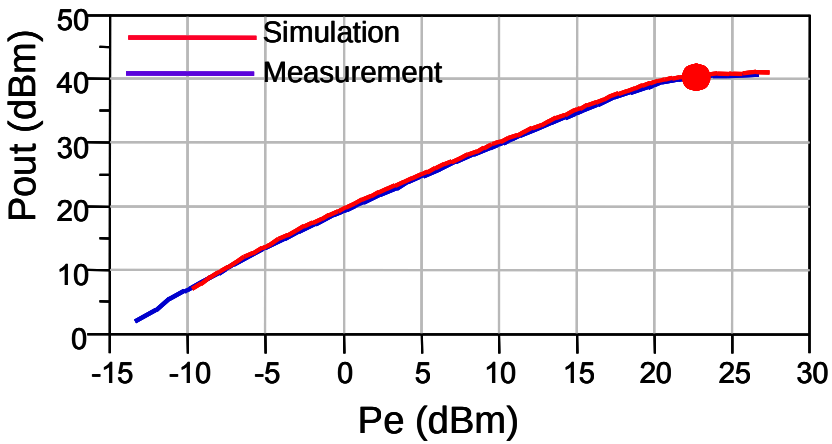
- ✓ V_{BK}>100V
- ✓ Rdson~ 2 ohm
- ✓ Cds=0.9 pF
- ✓ Cgs= 8 pF
- ✓ Rg=0.5 ohm

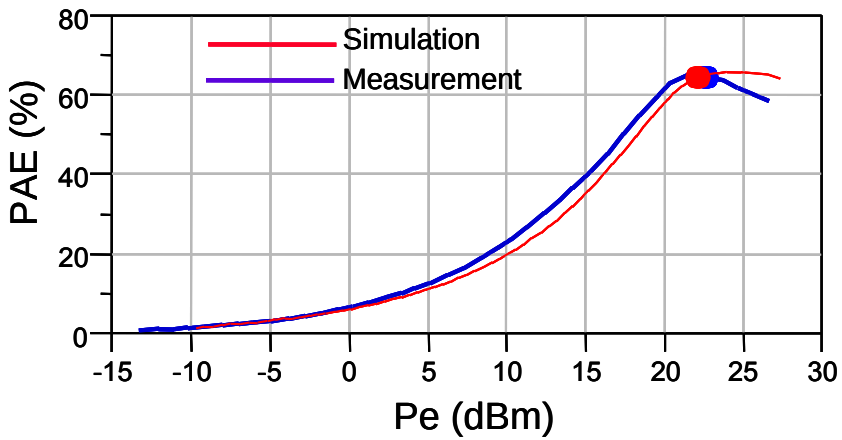
Device used : 15 W GaN HEMT from CREE CGH60015D

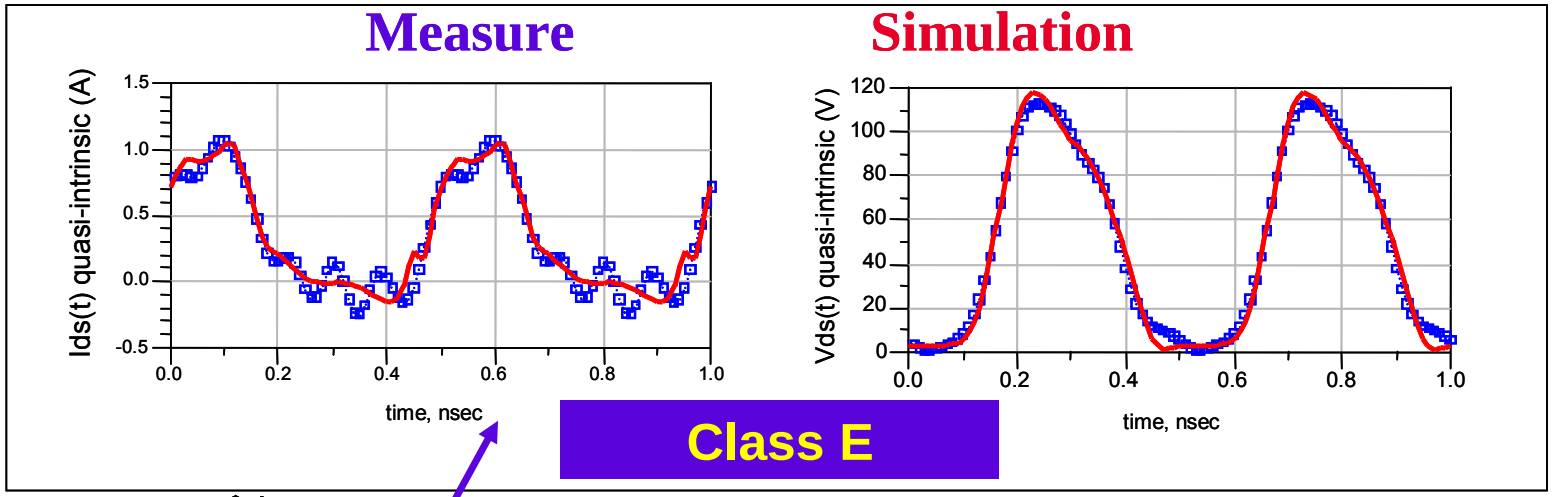
Device size 2mm

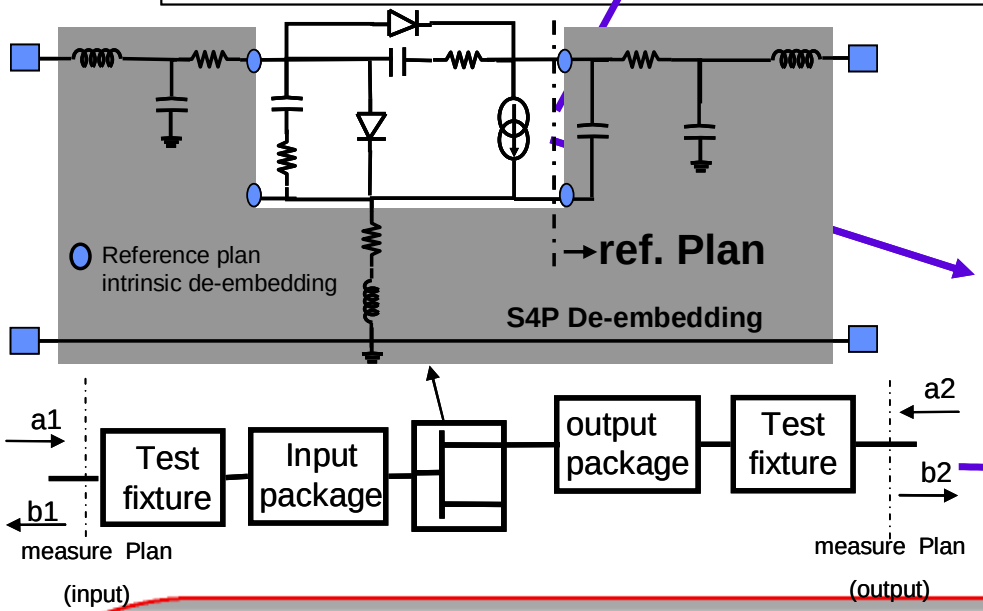
Test Jig and packaged transistor

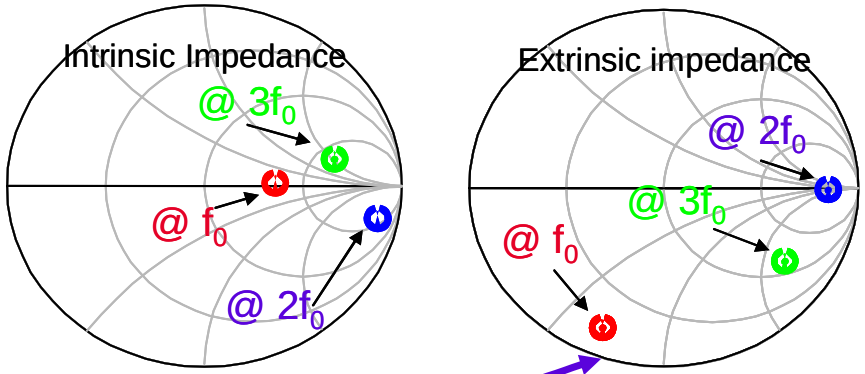


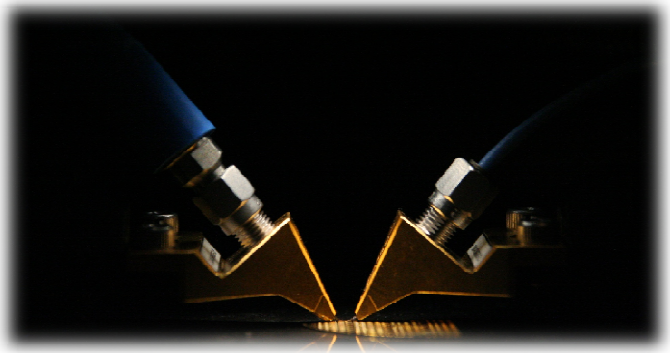





Measure
Simulation
Ids(t) quasi-intrinsic (A)
1.5
1.0
0.5
0.0
-0.5
0.0
0.2
0.4
0.6
0.8
1.0
time, nsec
Vds(t) quasi-intrinsic (V)
120
100
80
60
40
20
0
0.0
0.2
0.4
0.6
0.8
1.0
time, nsec
Class E


Reference plan
intrinsic de-embedding
→ref. Plan
S4P De-embedding
a1
b1
Test fixture
Input package
output package
Test fixture
a2
b2
measure Plan
(input)
measure Plan
(output)


Intrinsic Impedance
@ 3f0
@ f0
@ 2f0
Extrinsic impedance
@ 2f0
@ 3f0
@ f0

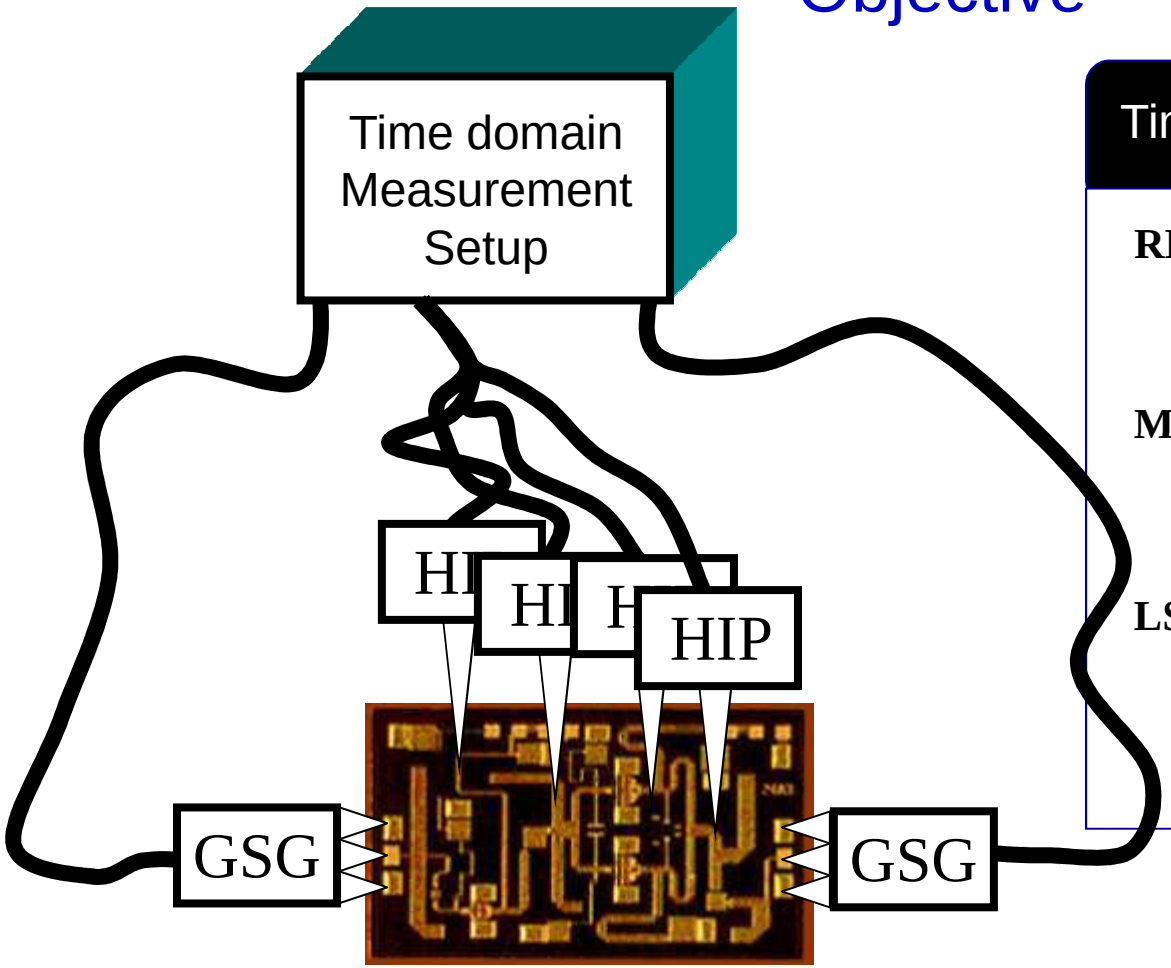


News trends

Time domain measurements for model validation

Time domain measurements for MMIC validation

Objective



MMIC

Time domain measurement system

RF sampling scope

- Long acquisition time
- Time base distorsions

MTA (Microwave Transition Analyser)

- Obsolete
- 2 channels

LSNA (Large Signal Network Analyser)

- Advanced technology (calibrated)
- 4 channels
- Commercialy available

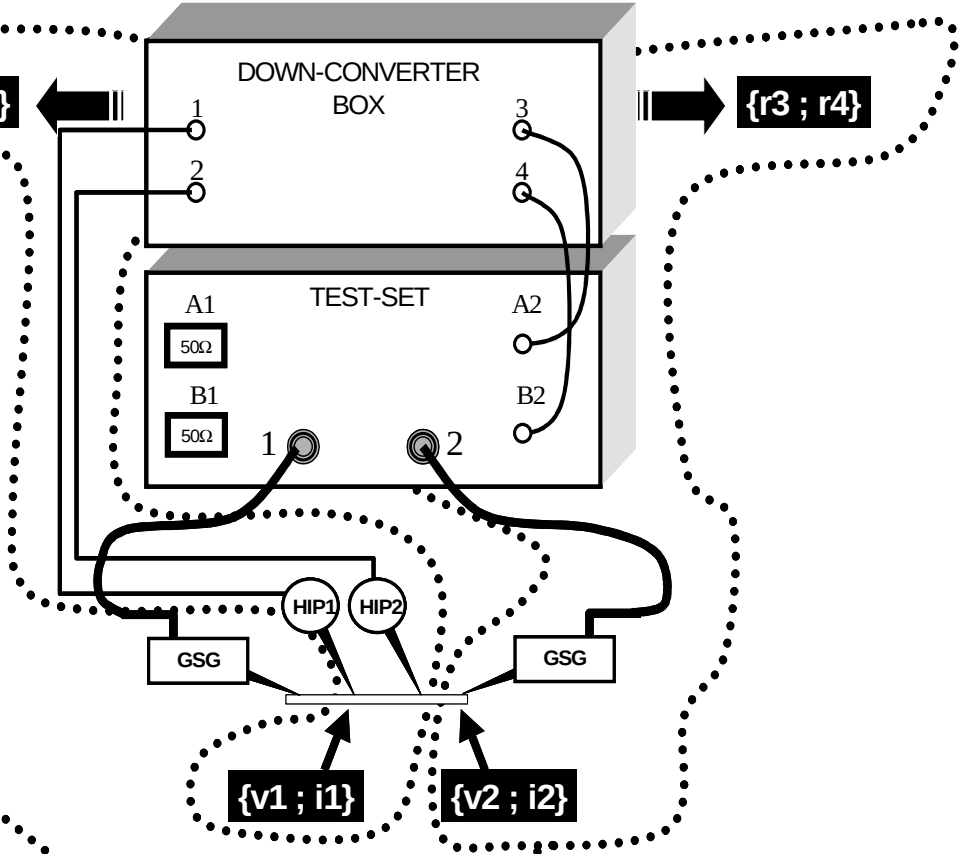
Configuration

HIP calibration assumption

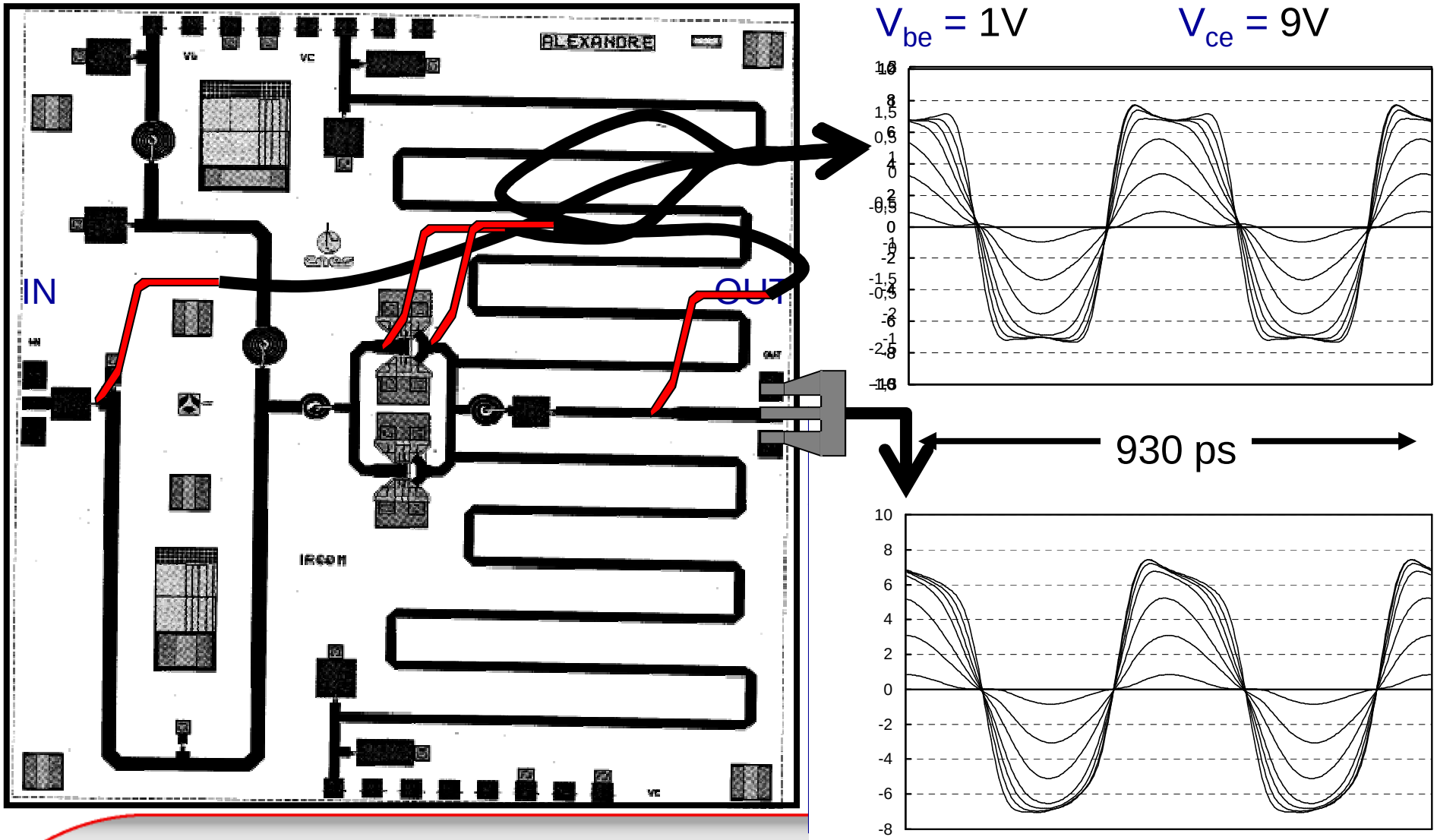
$$V_{ref.plane}(f) = \tilde{K}(f).V_{raw}(f)$$

Measurement Setup

$$\begin{pmatrix} v1 \\ i1 \\ v2 \\ i2 \end{pmatrix}_{LSNA} = \begin{bmatrix} \alpha_1^{HIP} & \beta_1^{HIP} & 0 & 0 \\ \gamma_1^{HIP} & \delta_1^{HIP} & 0 & 0 \\ 0 & 0 & \alpha_2^{CAL} & \beta_2^{CAL} \\ 0 & 0 & \gamma_2^{CAL} & \delta_2^{CAL} \end{bmatrix} \bullet \begin{pmatrix} r1 \\ r2 \\ r3 \\ r4 \end{pmatrix}_{LSNA}$$



Applications



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