Measurements for Optimization of Solid-State Power Amplifiers

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Introduction

Quick overview of classical measurement techniques for NL devices

Memory effects characterization and modeling

Waveform engineering based on measurements

Envelope tracking dynamical biasing / pre-distortion

High impedance probing

Conclusion
We all want more RF Power!
High power measurements can be funny

RF LDMOS – Bias Tee – Transmission line – Mismatched load

جامعاتنا جميعًا نريد المزيد من الطاقة RF!
قياسات الطاقة العالية يمكن أن تكون جنحة!

تتعارض الأجزاء مع بعضها البعض – خط الموجات – معادلة الأحمال.

هذا ليس بالضبط ما نريد، ولكن هناك الكثير من الطاقة RF هنا!)
Particular case of a nonlinear two-ports device with memory effects

4 instantaneous time-domain variables: $I(V)$ or $B(A)$

- **Device commands:** incident waves $a_1(t)$, $a_2(t)$
- **Device response:** reflected waves

\[
\begin{align*}
  b_1(t) &= f_{NL} \left[ a_1(t), a_2(t), \hat{a}_1(t), \hat{a}_2(t), \ldots \right] \\
  b_2(t) &= g_{NL} \left[ a_1(t), a_2(t), \hat{a}_1(t), \hat{a}_2(t), \ldots \right]
\end{align*}
\]

- **Instantaneous but recent history required**

- **Large number of terms for LF memory**

- **Signals with wideband modulations or large peak-to average are distorted**

- **These distortions are deterministic, we can compute then (with great efforts!)**
First-pass success of design / foundry process / tests of RF SSPAs

NL Meas. for modeling:
- Transistor Model
- Physical phenomena models
- Memory effects

NL Meas. for design:
- Wideband modulated signals
- Waveform engineering
- Envelope tracking data
- Pre-distortion data

NL Meas. for verification/debug:
- Specifications
- Performances
- Reliability
- High Impedance probing
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Motivation for short pulses: Control of the device self-heating

Fast behavior of GaN devices (thermal, traps): ultra short pulses <50ns required

Pulsed I(V) and Pulsed S-Parameters

Pulsed S-Parameter meas:
- linear elements
- nonlinear C(V)elements
- equivalent scheme model

Pulsed I(V) meas:
- I(V) characteristics
- Thermal characterization
- Trapping effects

Session 3: Characterization and modeling
Pulsed I(V) integrated systems available today

- Auriga/Diva AU4550
- Keithley 4200 SCS
- Agilent B1500A
- Amcad IVCad-PIV
- Focus Microwaves PIV
Measurement of highly mismatched power devices with large signals

Optimum impedances for:
- Output power
- PAE Max PAE
- Gain

Device performances
- C/I3
- ...

Possible improvements: pulsed or modulated signals, handling of harmonic frequencies
Direct access to source and drain time domain I(V) waveforms

- Model verification
- Waveform engineering
- Reliability (max slope)
- ...

Special features: Wave probes, NVNA receiver, multi-harmonic tuning, hybrid bias tees
<table>
<thead>
<tr>
<th>RF heads</th>
<th>Mixer-based</th>
<th>Sampler-based</th>
</tr>
</thead>
<tbody>
<tr>
<td>Downconversion</td>
<td>Agilent NVNA</td>
<td>Anritsu VectorStar + HFE</td>
</tr>
<tr>
<td>Frequency by frequency acquisition</td>
<td>R&amp;S ZVA+ NMDG</td>
<td>VTD SWAP X402 (formerly the MTA, the LSNA)</td>
</tr>
<tr>
<td>(needs a phase reference gen.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>One-shot acquisition of all frequencies</td>
<td>Impossible</td>
<td></td>
</tr>
<tr>
<td>(a sampler as phase reference)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Sampler-based NVNA wideband down-conversion principle

\[ f_{IF} = f_{RF} - N \frac{f}{\frac{1}{\tau}} \]

A NVNA features 4 identical channels
(6 are possible for special needs like frequency conversion devices)
The sampler technique allows extreme pulse mode (50ns, 0.01%)
NonLinear behavior of RF power amplifiers when a modulated signal is applied

 Needs a specific and complex calibration procedure
Measurements from 10 Hz to 40 GHz

Special low frequency bias tees have been designed
Quick overview of possible test signals

- **Simple RF test signals:**
  - one-tone (CW):
    - S-parameters, AM/AM and AM/PM, constant envelope
    - Waveform distortion, compression
  - 2-tones, 3 tones:
    - Intermodulation C/I, IP, LF memory, variable envelope, peak to average
    - Envelope distortion

- **Complex RF test signals:**
  - Multitone signals:
    - Noise Power Ratio
    - Signal distortion
  - Modulated carrier:
    - Adjacent Channel Power Ratio
    - Dynamical behavior of NonLinearities
Tentative chart of RF measurement instruments

Frequency domain
- Vector Network analyzers
- Scalar networks
  - Spectrum analyzers
  - Powermeters

Time domain
- NVNA
  - Sampling Scopes
  - VSA

Ease of use
- Simple
- Complex

Power detection
- Fast Arbitrary Wave Generator

Information
- Poor
- Large

New!

- Absolute power
- Harmonic distortion
- Image reject
- Oscillator stability
- Intermodulation
- NPR / ACPR

- [S] CW
- [S] pulsed
- Gain
- Linearity
- SWR
- Compression
- Impedance
- Group delay
- Isolation
- Pulse profile

- Distortion
- Time domain
- Error rate
- Modulation
- Eye diagram
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Discrepancy between DC and RF behavior

Gm at point A versus measurement conditions

\[
\begin{align*}
G_{m(A)}^\text{dc} &= f(V_{gsA}, V_{dsA}, \text{TrapsA}, TA) \\
G_{m(A)}^\text{PIV} &= f(V_{gsA}, V_{dsA}, \text{TrapsB}, TB) \\
G_{m(A)}^\text{RF} &= f(V_{gsA}, V_{dsA}, \text{TrapsC}, TB \& PAE)
\end{align*}
\]

We get 3 very different values of Gm. \( Y21 \neq dI/dVDS \)

Consequences of low frequency memory effects on drain current

(thermal effect and trapping effects)
Bias current versus input power (1/4)

- $20\text{ T10 T5 0 5 10 15 T15 20}$
- $180 \quad 200 \quad 160 \quad 220$
- $\text{IDS (mA)}$
- $\text{Pin (dBm)}$
- $180 \text{ mA}$
- $\text{Drain-lag status}$

Vienna, April 18th-19th, 2011
Bias current versus input power (2/4)
Bias current versus input power (3/4)

- **IDS (mA)** vs **Pin (dBm)**
  - IDS = 220 mA at Pin = -15 dBm
  - IDS = 160 mA at Pin = 20 dBm

- **Drain-lag status**
  - Vds = 165 mA
The drain-lag traps are filled by VDS maximum value, even at RF frequencies.
Effect of PIV DC point on I(V) characteristics

The device temperature is identical, thus the discrepancy is due to drain lag effects.

The PIV measurements put in evidence trapping memory effects.

\[ V_{ds0} = 12V \]
\[ I_{ds0} = 30 \text{ mA} \]

\[ V_{ds0} = 4V \]
\[ I_{ds0} = 90 \text{ mA} \]
GaN 8x75 µm, Pulses 700ns, Period 1ms, hot biasing point

-20 °C
25 °C
100 °C

Biasing point (start of pulses)

Vgs0= +2V
Vgs0= 0V
Vgs0= -1V
Vgs0= -1.5V
Vgs0= -2V
Vgs0= -5V
GaN 8x75 μm, Pulses 700ns, Period 10 μs, cold VDS0=0 biasing point

Trap capture and emission time constants are varying versus temperature: Arrhenius
GaN 8x75 μm, Pulses 700ns, Period 10 μs, cold VDS0=0, VGS0=0 biasing point

Kink effect only at intermediate temperatures
GaN 8x75 μm, Pulses 700ns, Period 10 μs, cold VDS0=0, VGS0=0 biasing point

This effect is explained by the temperature dependance of trap emission time constant
Ron and Idss measurements at different base-plate temperatures

Pulsed I-V characteristics ($V_{GS} = 0$ V) from zero power bias point ($V_{DS0} = V_{GS0} = 0$ V)
Ron and Idss measurements for different dissipated power

Pulsed I(V) characteristics ($V_{G_S i} = 0$ V) from various quiescent bias points ($V_{G S 0} = 0$ V, $V_{D S 0} = 2\text{–}13.5$ V) with fixed thermal chuck at 25 °C.
The Thermal Resistance is the ratio between the Ron slopes

\[ R_{ON}(\Delta T) = R_{ON}(T_0) + \frac{dR_{ON}}{dT} \cdot \Delta T \]

\[ R_{ON}(P_{diss}) = R_{ON}(0) + \frac{dR_{ON}}{dP_{diss}} \cdot P_{diss} \]

- \( T_0 = 25 ^\circ C \)
- \( \Delta T = T - T_0 \)

\[ R_{TH} = \frac{\Delta T}{\Delta P_{diss}} = \left( \frac{dR_{ON}}{dP_{diss}} \right) \cdot \left( \frac{dR_{ON}}{dT} \right) \]

😊 Self-heating during pulses is not an issue because we extract a slope
Classic flow-chart of RF transistor NL modeling

Session 3: Characterization and modeling
Dynamical thermal behavior

3-D Thermal simulation

Heating versus time

\[
\text{TEMP} = 22.8 \times (1-e^{-t/\tau_1}) + 21.7 \times (1-e^{-t/\tau_2}) + 7 \times (1-e^{-t/\tau_3}) + \ldots
\]

Thermal equivalent circuit for simulation
This is a possible FET model amongst many “good agreement” or improved models!

Such a model cannot be perfect everywhere, the targeted application must be considered
The trap effects on drain current are taken into account by a modified VGS (Vgs_int).

Note the unsymmetrical capture and emission effects modeled by the envelope detector.
Conclusions on LF memory effects

- We have shown some electrical effects of LF memory effects, there are many others:
  - at circuit level when large peak to average are applied
  - at system level (Bit Error Ratio)
  - phase shifts are to be considered for RADAR applications…
- We have shown some techniques to characterize LF memory effects
  - a lot of work is carried out in labs to find reliable techniques to separate trapping and thermal effects (same frequency range)
  - fast pulses and very low frequency measurements are interesting ways
- We have shown some possible modeling approach based on equivalent circuit
  - Many model topologies, equations and methods are available
  - With improved Volterra models (like X-Parameters), long-term memory effects can now be taken into account with models driven by meas. data
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Simplified GaN HEMT model

Minimization of dissipated power:
- During ON state $V_{ds}$ must be minimum $\Rightarrow$ Low $R_{ds, on}$
- During transitions $\frac{dV_{ds}}{dt}$ and $\frac{dI_{ds}}{dt}$ must be maximum $\Rightarrow$ Low capacitances ($C_{gs}, C_{ds}$)

Waveform engineering to increase PAE
Control the Gate source waveform shape

Source network

Load Network

Vgs(t)

Ids(t) Vds(t)

Aperture angle reduction

Second Harmonic injection

\[ V_{gs}(t) = V_{gs0} + V_{gs1} \cos(wt) + V_{gs2} \cos(2\cdot wt + \phi) \]

\[ V_{gs2} = \frac{V_{gs1}}{7}, \phi=0 \]
PAE enhancement by gate source voltage shaping

Two stage PA design

Input Matching at f0

Interstage Matching at f0, 2f0, 3f0

Output Matching at f0, 2f0, 3f0

\[ V_{gs0,1} = -2.0V \]
\[ V_{ds0,1} = 7V \]
\[ V_{gs0,2} = -2.3V \]
\[ V_{ds0,2} = 28V \]

\[ R = 500 \Omega \]

\[ Q_1 \quad Q_2 \]

\[ V_{gs}, d \]
\[ V_{ds}, d \]
\[ V_{gs}, p \]
\[ V_{ds}, p \]

\[ C_d \]

\[ 50\Omega \]

(a) Reducing of t_on

\[ V_p \]

(b) Vgs intrinsic

\[ 0.0 \quad 0.2 \quad 0.4 \quad 0.6 \quad 0.8 \quad 0.0 \quad 1.0 \]

\[ V_{on} \quad V_{off} \]

\[ 0.0 \quad 0.2 \quad 0.4 \quad 0.6 \quad 0.8 \quad 1.0 \]

\[ 0.0 \quad 10 \quad 20 \quad 30 \quad 40 \quad 50 \quad 60 \]

\[ V_{ds} \quad \text{intrinsic} \quad (A) \]

\[ 0.0 \quad 0.2 \quad 0.4 \quad 0.6 \quad 0.8 \quad 1.0 \]

\[ 0.0 \quad 2.0 \]

\[ V_{gs} \quad \text{intrinsic} \quad (V) \]
Time domain measurements at internal nodes

High impedance probing for waveform checking and tuning
Comparison with a conventional class F design

Single Stage conventional class F PA (PA1)

Two Stage PA with gate source voltage waveform shaping (PA2)
Measurement results at connector ports

Comparison between single and two stage Power Amplifiers (same foundry)
Large Signal Measurement results at 4 dB gain compression
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High Efficiency ⇒ Power amplifier architectures based on dynamic biasing techniques

Linearity ⇒ Power amplifier architectures based on digital pre-distortion

⇒ Development of Specific test-bench

- Identify dynamic drain bias law in presence of memory effects.

- Apply both Envelope Tracking (ET) and Digital Pre-Distortion (DPD) techniques.

- Maximize both PAE and linearity.

Clock synchronization and envelope trigger signals are carefully controlled
Appropriate time alignment between RF signal envelope and drain bias signal are achieved
Modulated signal is applied to the PA input (QAM16 in the present case).

Fixed DC voltage is applied to the drain bias port.

Instantaneous input/output envelop transfer functions are recorded.

The coordinates of the targeted drain bias law are taken to keep constant saturated gain and high drain efficiency.
Application of drain bias law (100 KHz 16-QAM)

GaN CREE 10 W @ 3.6 Ghz
(Vgs=-2.65 V, Ids= 190 mA @ 28V)

Large capacitances of the drain bias circuit are removed
A simple first order base band predistorsion technique
- It consists in extracting spline functions fitting the average of measured dynamic AM/AM and AM/PM characteristics of the ET amplifier, and inverting them
- Can be improved (DSP, FPGA) to consider LF memories
OFDM Signal 128 sub carriers 16QAM at 1MBit/S
Oversampling Ratio=4  Fe=4MHz

GaN CREE 10 W @ 3.6 Ghz ( Vgs0=-2.65 V , IdsQ= 190 mA @ 28V)

Main effect of Envelope Tracking (ET)
Main effect of Digital PreDistortion (DPD)
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Motivations for High Impedance Probes (HIP)

Time domain Measurement Setup

HIP

GSG

MMIC
HIP calibration assumption

Measurement Setup

\[
\begin{pmatrix}
  v_1 \\
  i_1 \\
  v_2 \\
  i_2
\end{pmatrix}_{LSNA} =
\begin{pmatrix}
  \alpha_{\text{HIP}} & \beta_{\text{HIP}} \\
  \gamma_{\text{HIP}} & \delta_{\text{HIP}} \\
  0 & 0 \\
  0 & 0
\end{pmatrix}
\begin{pmatrix}
  r_1 \\
  r_2 \\
  r_3 \\
  r_4
\end{pmatrix}_{LSNA}
\]

\[
V_{\text{ref. plane}}(f) = \tilde{K}(f) \cdot V_{\text{raw}}(f)
\]
1. NVNA calibration (LRRM)

\[
\begin{pmatrix}
 v_1 \\
 l_1 \\
 v_2 \\
 i_2
\end{pmatrix}_{LSNA} = \begin{bmatrix}
 \alpha_1 & \beta_1 & 0 & 0 \\
 \gamma_1 & \delta_1 & 0 & 0 \\
 0 & 0 & \alpha_2 & \beta_2 \\
 0 & 0 & \gamma_2 & \delta_2
\end{bmatrix}
\begin{pmatrix}
 r_1 \\
 r_2 \\
 r_3 \\
 r_4
\end{pmatrix}_{LSNA}
\]

→ Ref. plane = voltage standard

2. Calibration with 1 HIP

- HIP @ ref. plane
- « Sweep-sin »
- Measurements :
  > \(v_2\) (NVNA calibrated)
  > \(v_{HIP}\) (raw data)

\[
\tilde{K}(f) = \frac{v_2(f)}{v_{HIP}(f)}
\]

3. Define a new error-matrix (NVNA + 2 HIPs)

**Measurement of 2 voltages (M1)**

\[
\begin{pmatrix}
 v_1 \\
 l_1 \\
 v_2 \\
 i_2
\end{pmatrix} = \begin{bmatrix}
 \tilde{K}_1 & 0 & 0 & 0 \\
 0 & \tilde{K}_2 & 0 & 0 \\
 0 & 0 & \alpha_2 & \beta_2 \\
 0 & 0 & \gamma_2 & \delta_2
\end{bmatrix}
\begin{pmatrix}
 r_1 \\
 r_2 \\
 r_3 \\
 r_4
\end{pmatrix}
\]

\(v_1(t) \Leftrightarrow v_1(t)\)
\(i_1(t) \Leftrightarrow v_2(t)\)
HIP measurement applications (1/2)

- \( V_{be} = 1V \)
- \( V_{ce} = 9V \)

930 ps
1. MMICs validation

2. Stability

HIP enables easy detection of oscillations

NVNA enables phases measurements

KNOWLEDGE OF NONLINEAR PHENOMENA

OPTIMAL DESIGN FOR POWER AMPLIFIERS

Spectral Analysis

OUTPUT of a Power Amplifier

CW Stimulus @f₀
HIP + NVNA open the way to measurement-based waveform engineering of SSPAs

**Analysis…**
**Identification…**
**Understanding…**

**DYNAMICS**
**NONLINEAR**
**PHENOMENA**

**SIMULATIONS**
- Time Domain Integration
- Harmonic Balance + Envelope Transient

**MEASUREMENTS**
- Time Domain Characterization
- NVNA + HIP

**Optimized designs of MMICs**
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Conclusions

- NonLinear measurement of RF active devices are mandatory
  - for transistor test, modeling and model verifications
  - for memory effects identification
  - for direct optimization of SSPAs
  - for reliability investigations
  - ....

- Research is still going on
  - New ways to separate and accurately measure LF memories
  - New measurement instruments, new set-ups
  - Cost of NL measurements is to be considered (Return On Invest)
  - We estimate that clever NL meas. are the best way for SSPA 1st pass success

A lot of research on RF NL topics (measurement, modeling, instrumentation…) is carried out in Europe. Here in Vienna it’s the good place to thank again the TARGET Network of Excellence for its invaluable support.