High efficiency two stage microwave GaN power amplification with gate source waveform shaping of the power stage

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High Efficiency Power Amplifiers : analogue-digital balance - W 08 –(EuMC/EuMIC)

Outline

i. **Introduction**

ii. **Principle of gate source voltage waveform shaping**

iii. **One stage and two stage PA designs (comparative results)**

iv. **Conclusion**

i- Introduction

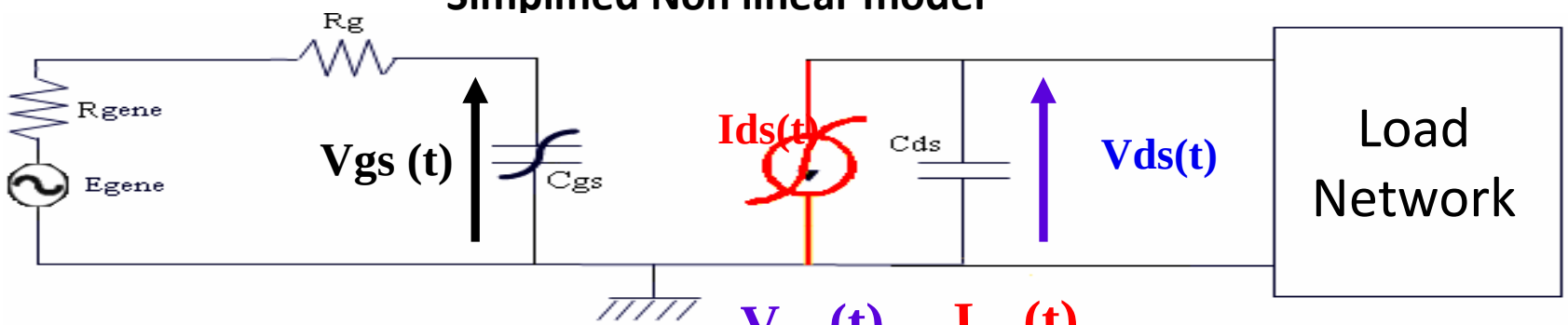
High efficiency power amplification

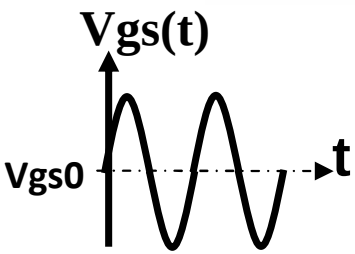
Signals	Constant enveloppe	Variable envelope
Spectral efficiency	low	High
Linearity requirement	No	High (linéarisation is often needed)
Application	✓ Radar ✓ Radionavigation , …..	✓ Télécommunications

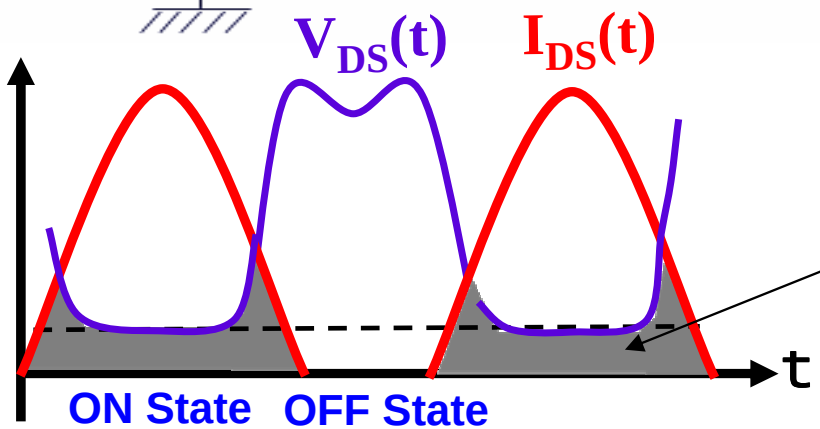
The highest PAE over the widest bandwidth is required

High efficiency operating conditions of transistors at microwaves

Simplified Non linear model







Shaded area indicating dissipated power

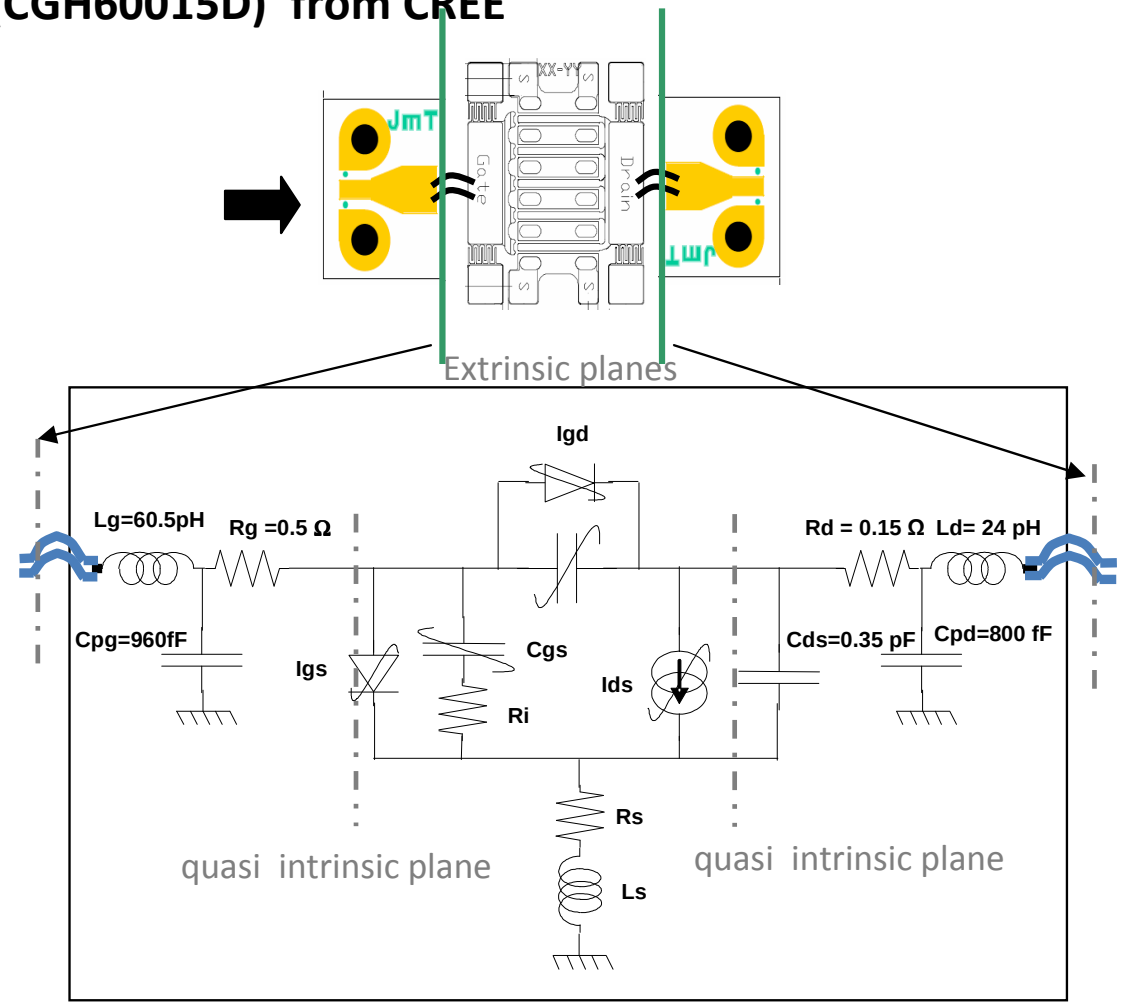
- Minimisation of drain current and drain voltage overlap at intrinsic port
- High power at microwaves - High voltage operation - → **GaN devices : good candidates**
- Amongst major features/challenges are : minimise power loss at output combination & gate source drive for power devices (RC input low path behavior)

ii- Gate source voltage waveform shaping

Non linear model topology

Device used in this study :GaN HEMT 15W(CGH60015D) from CREE

- ✓V_{BK}>120V
- ✓Rdson~ 3 ohm
- ✓Cds=0.35 pF
- ✓Cgs= 6.5 pF
- ✓Rg=0.5 ohm

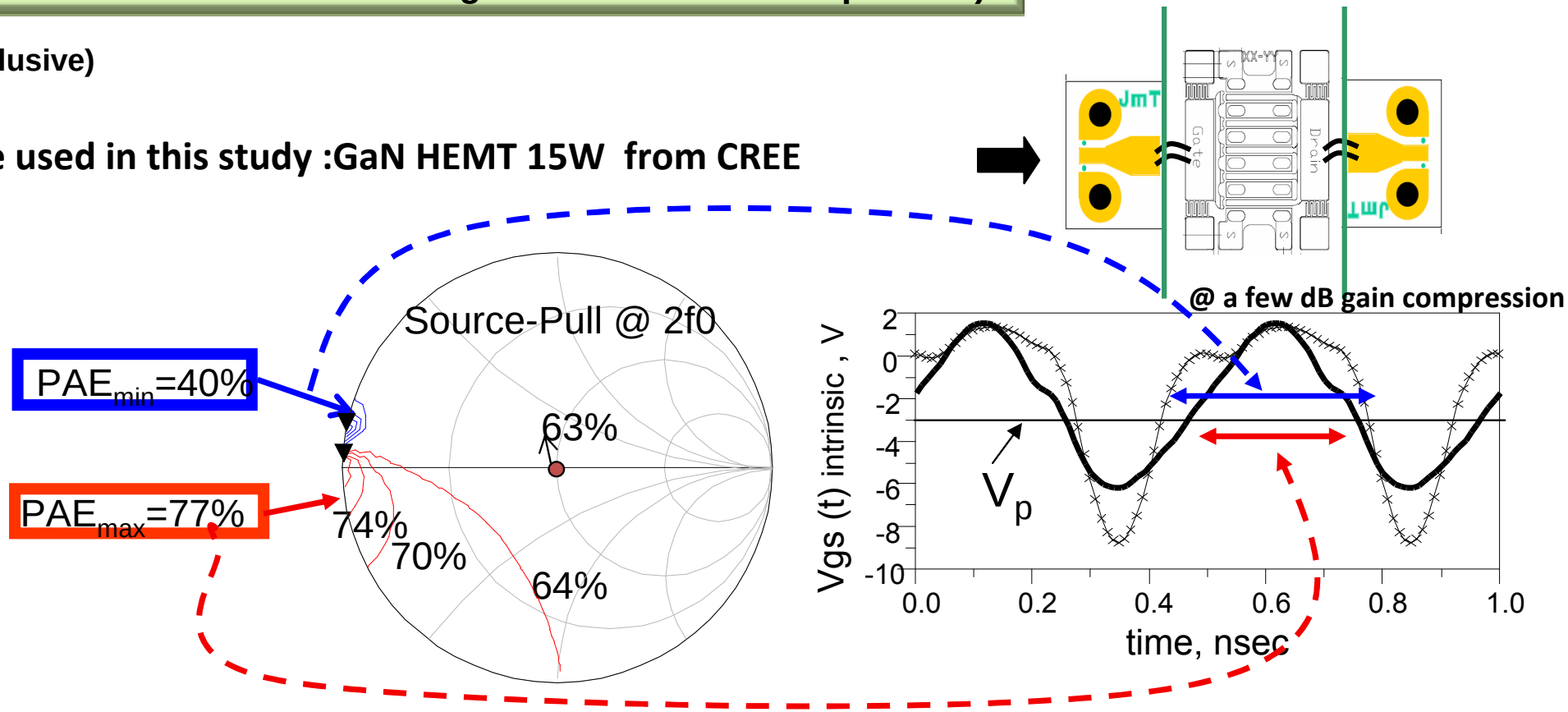


Source-pull simulation at harmonic 2 : (Fundamental F0 =2 Ghz)

(In the present case : classe F matching conditions at the output **)

** (it is not exclusive)

Device used in this study :GaN HEMT 15W from CREE



➢IF Gate source voltage shape is enlarged in the area above Pinch Off voltage- PAE decreases dramatically (Important aspect for high PAE over wide bandwidth)

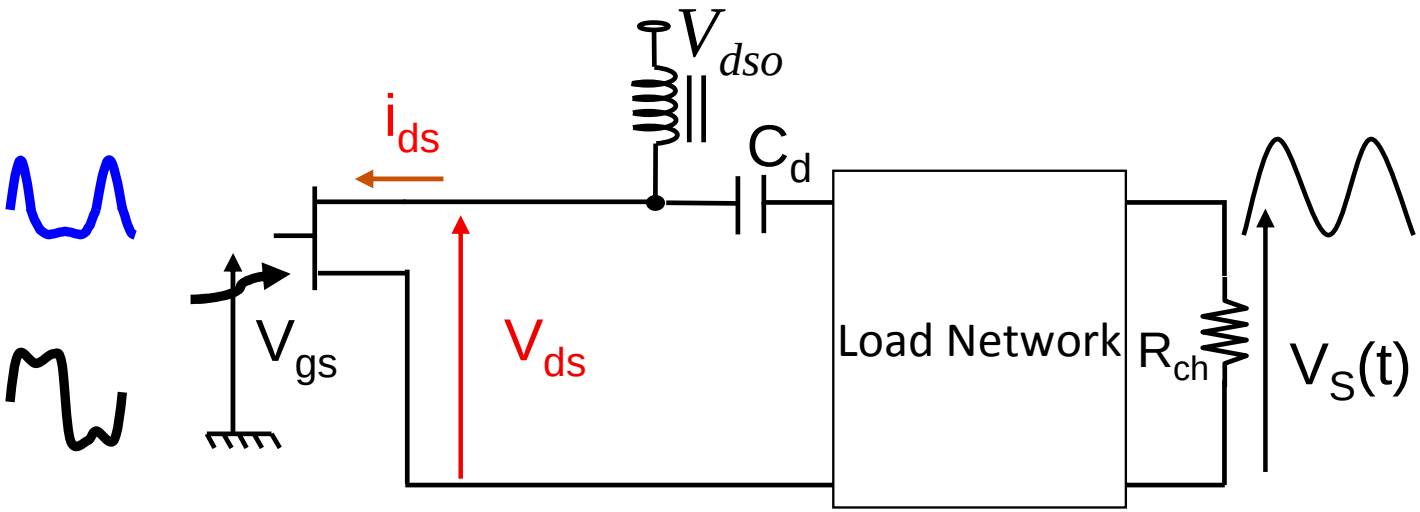
Active second harmonic injection is studied (First 3 harmonic components)

(1) ➢ half sine wave shape

(H2 is needed)

(2) Quasi-square wave

(H3 is needed)

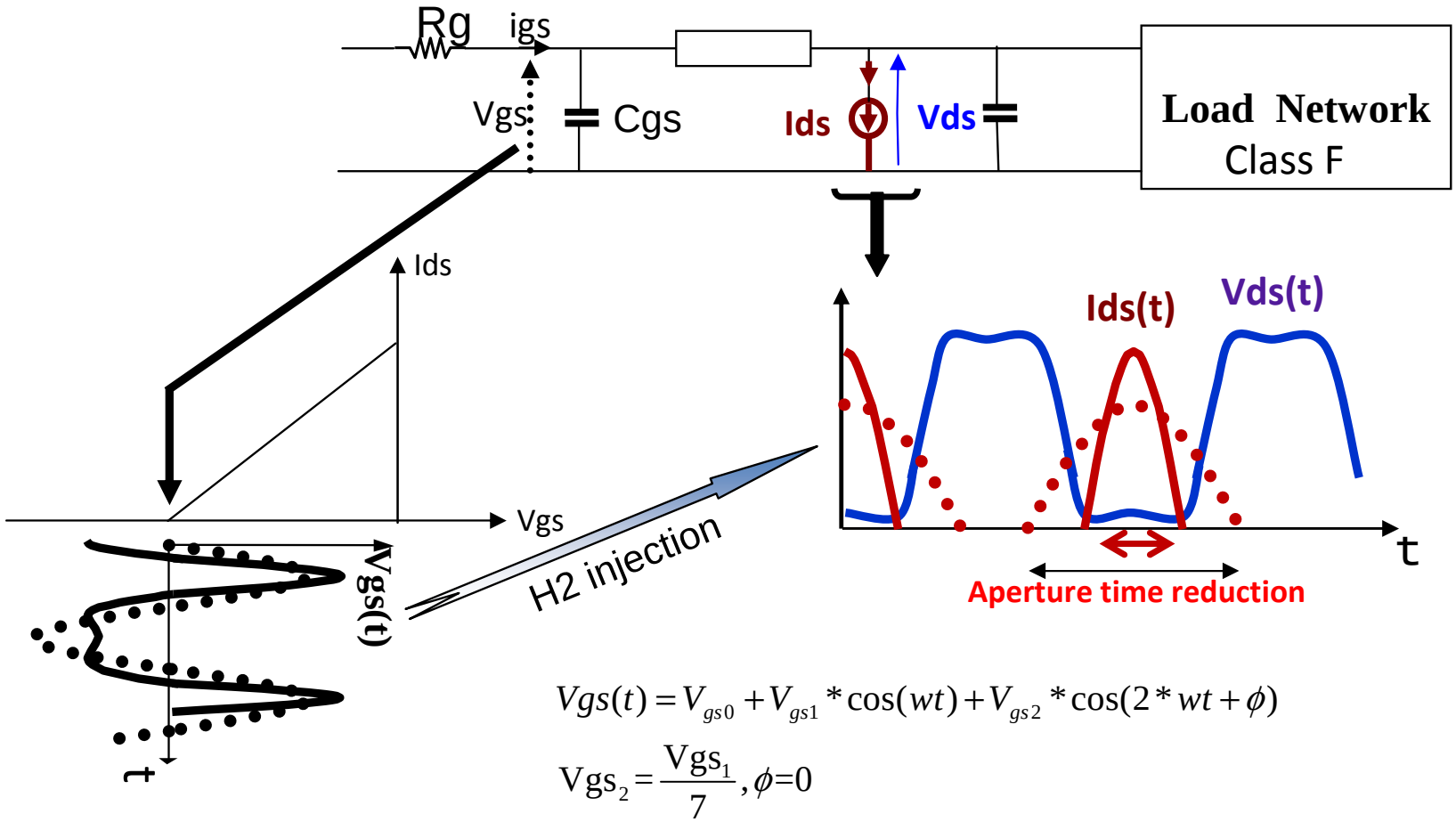


➢With (1) ➡ Low impedance output matching conditions at H2

➢With (2) ➡ Low impedance output matching conditions at H3

Case (1) has been adopted here
Half sine wave gate source voltage + Classe F output matching conditions

Half sine wave shape of Vgs leads to aperture time reduction

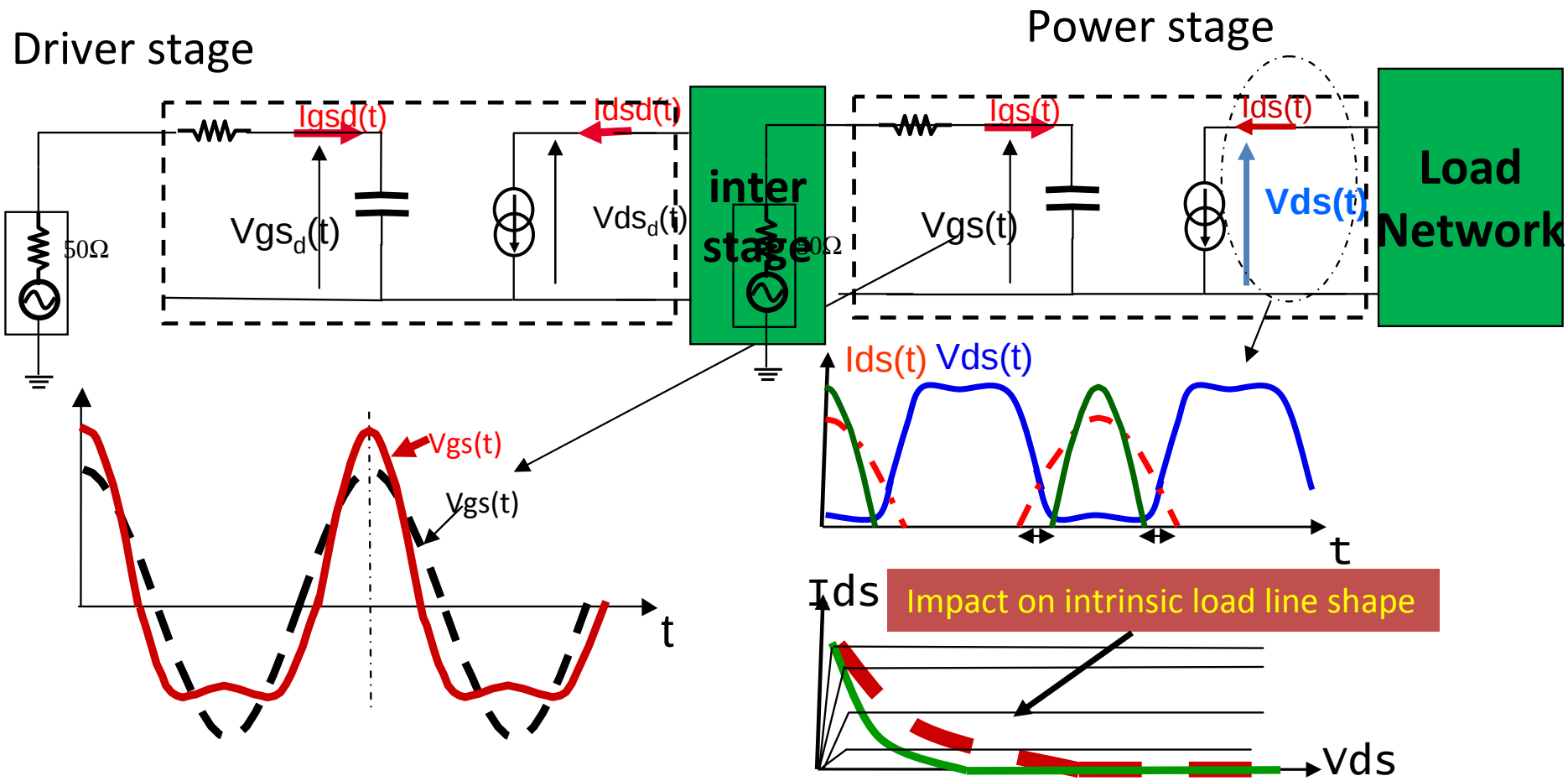


$$Vgs(t) = V_{gs0} + V_{gs1} * \cos(wt) + V_{gs2} * \cos(2 * wt + \phi)$$

$$\mathrm{Vgs}_2 = \frac{\mathrm{Vgs}_1}{7}, \phi = 0$$

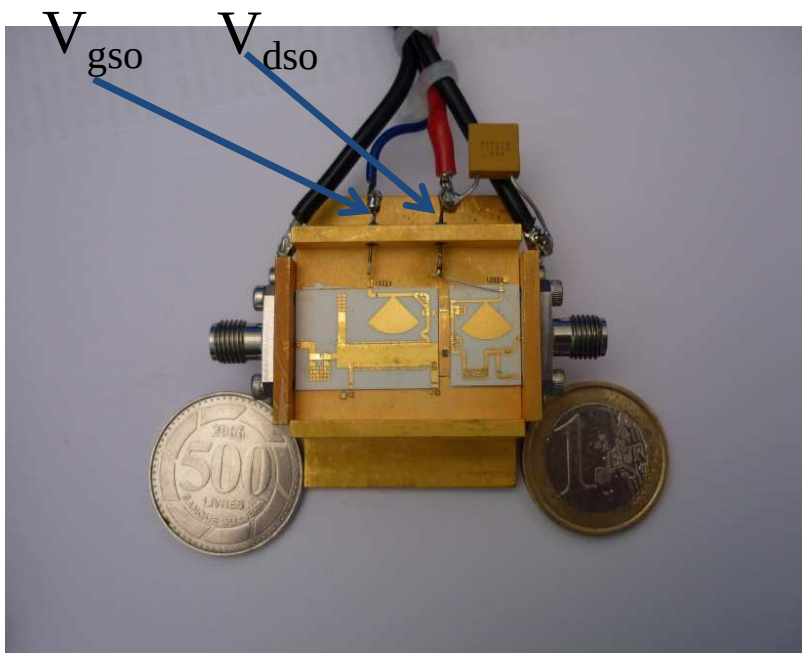
➢ **Appropriate H2 injection conditions are indirectly observable on a decrease of DC drain current Ids0**

Driver stage and power stage association (principle)



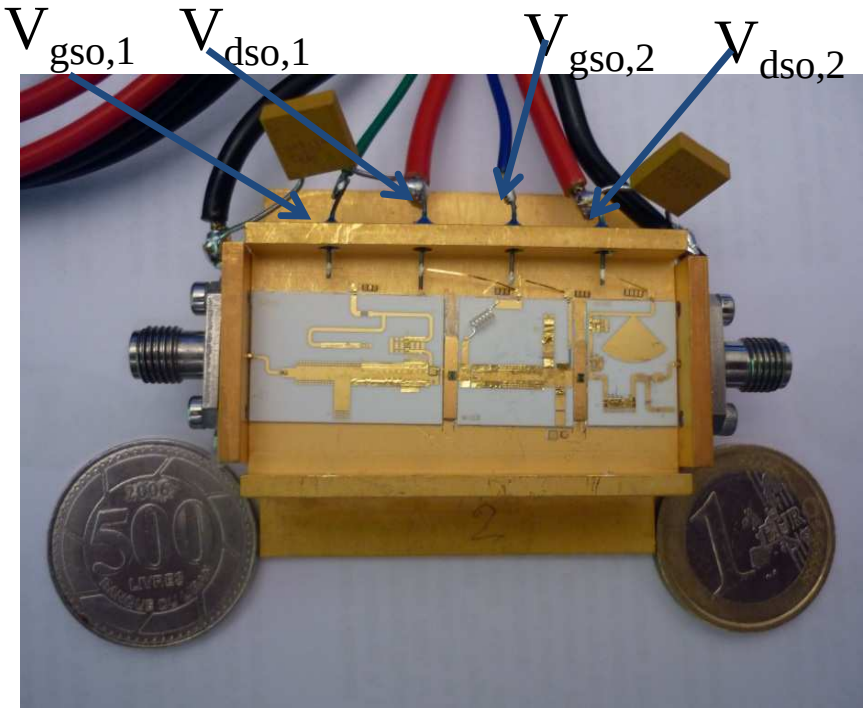
iii-One stage and Two stage PA Designs

Two PA Designs for Comparative Results



One Stage ClassF PA

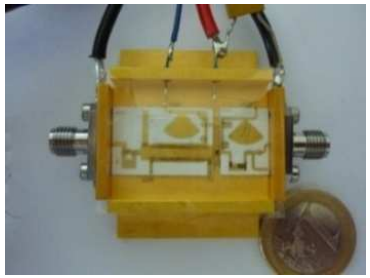
(PA1)



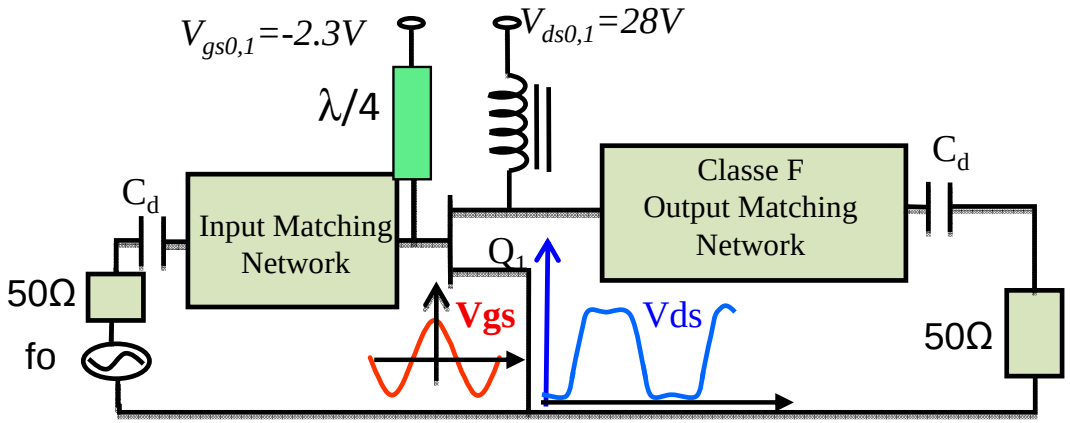
Two Stage PA:
(Driver + ClassF power stage)

(PA2)

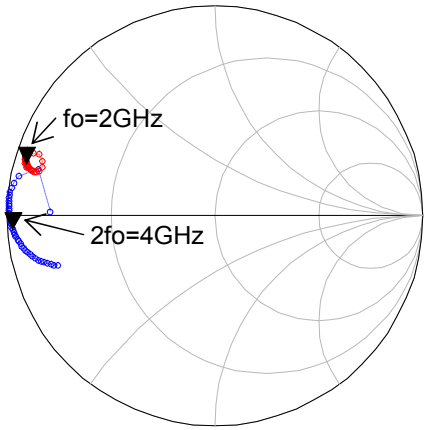
One stage Class F PA (PA1)



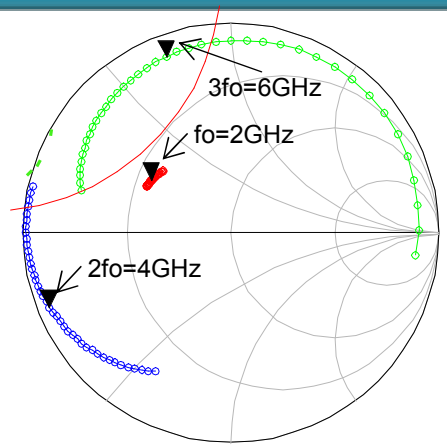
(PA1)



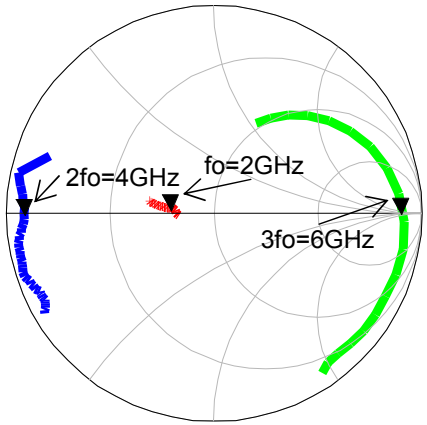
Extrinsic Source Impedance @fo &2 fo Vs freq



Extrinsic Load impedances @ fo, 2fo et 3fo Vs freq

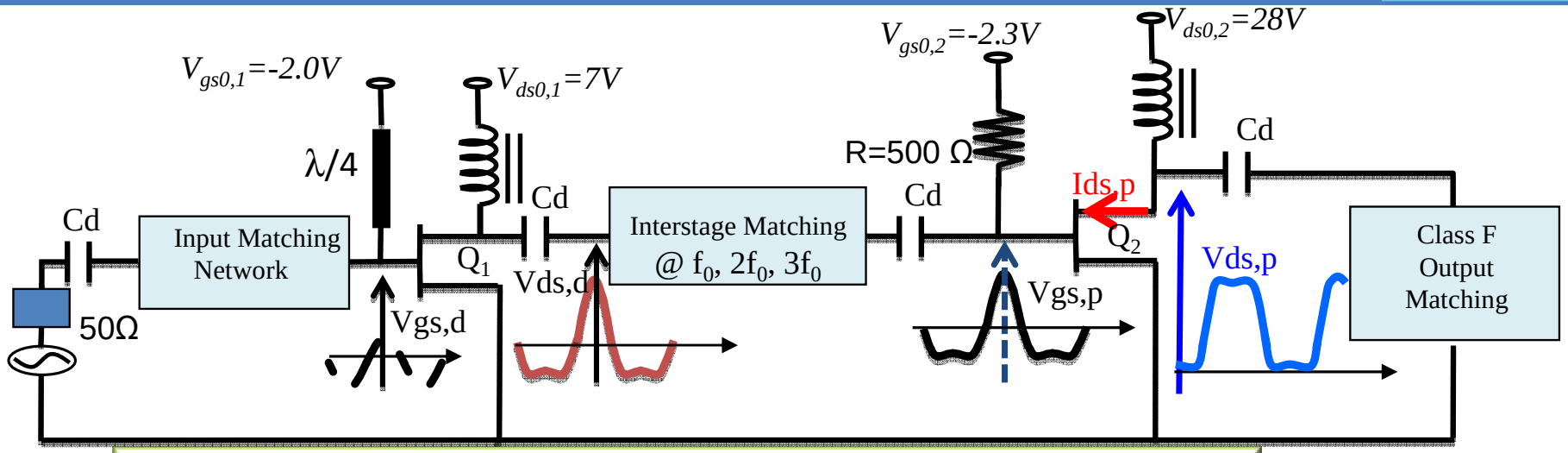


Intrinsic Load impedances @ fo, 2fo et 3fo Vs freq



Frequency Sweep (1.8GHz-2.2GHz)

Two stage PA (PA1)



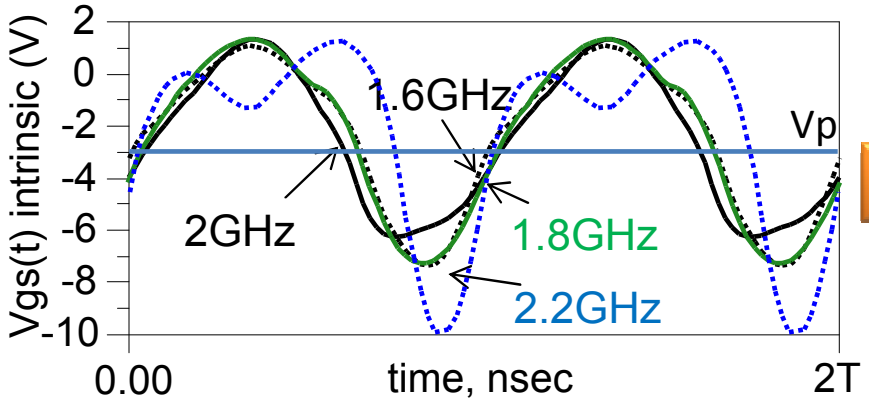
Few design aspects

(1) No λ/4 line at drain bias network of the driver and at gate bias network of power stage

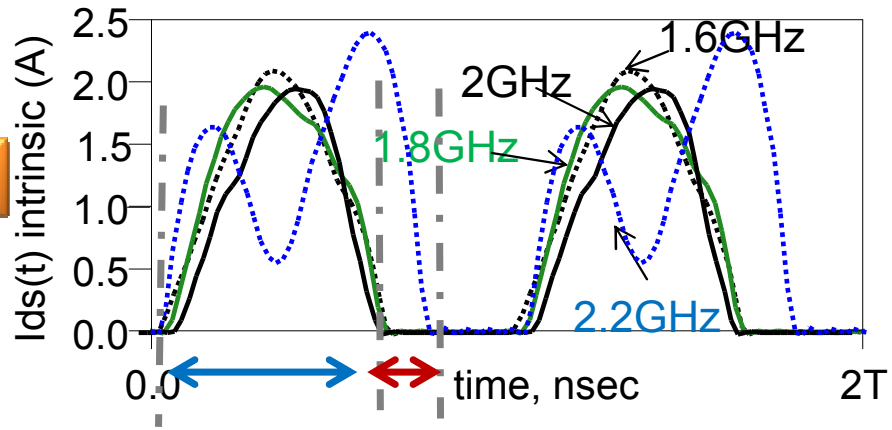
(2) Q1 (driver) operates at low Vds0 (7V) under class F^{-1} operation

(3) Interstage matching: trade off between power matching and voltage matching .

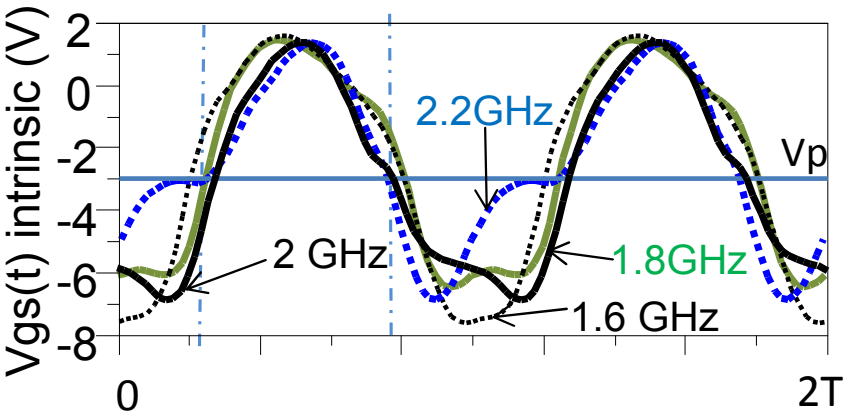
Voltage and Current Waveforms of the power stage (Simulated Results)



One stage PA1

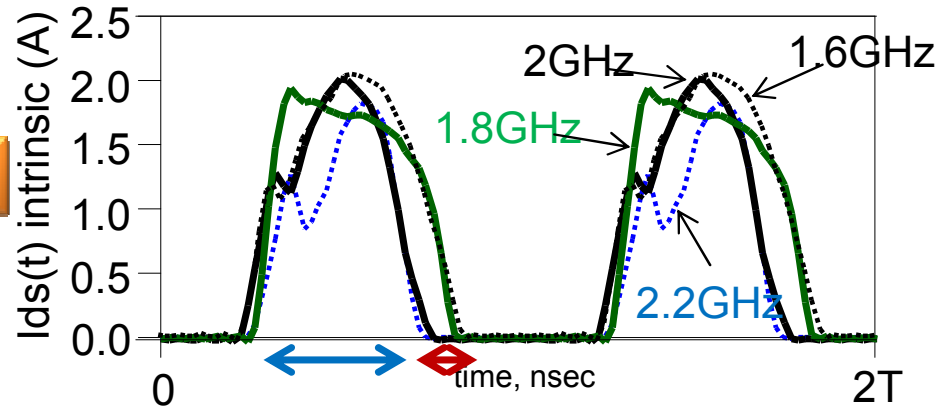


Gate source voltage Waveform



Two stage PA2

Drain current Waveform

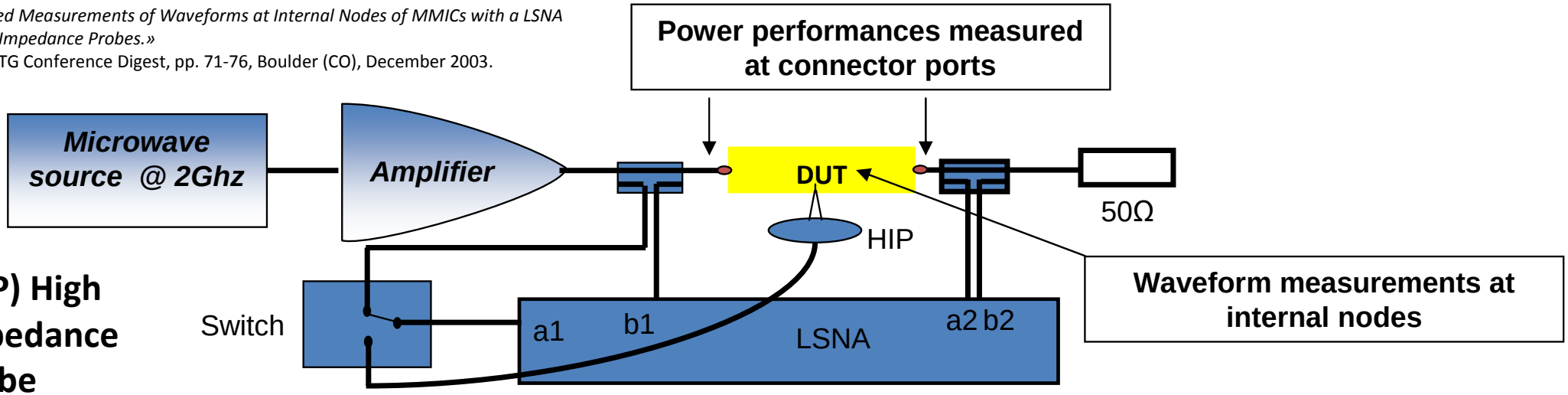


Limited scattering of aperture time

Validation of the study by Time domain waveform measurements

T. Reveyrand, A. Mallet, J.M. Nébus, M. Vanden Bossche

«Calibrated Measurements of Waveforms at Internal Nodes of MMICs with a LSNA and High Impedance Probes.»
62nd ARFTG Conference Digest, pp. 71-76, Boulder (CO), December 2003.

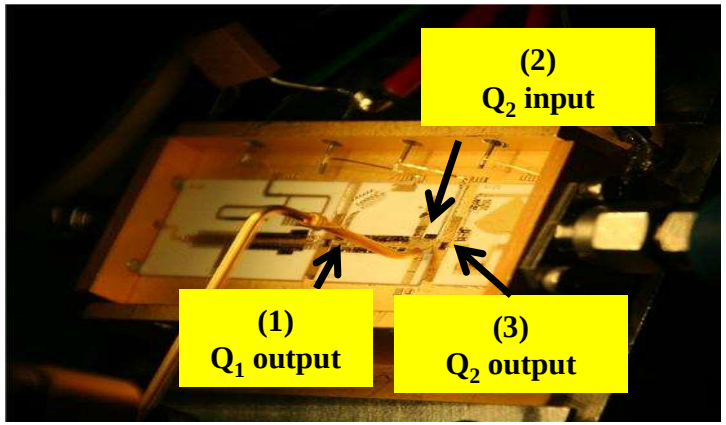


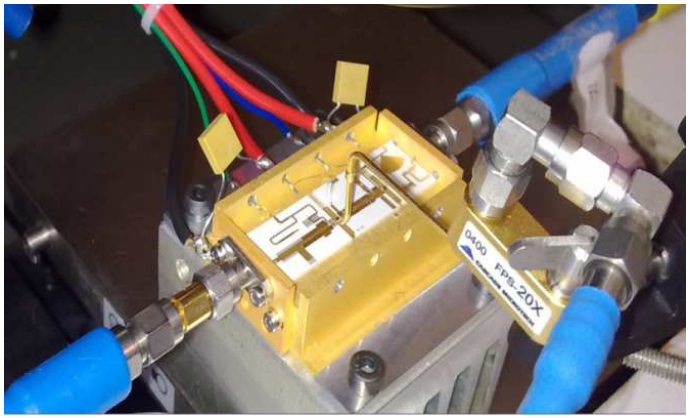
(HIP) High Impedance Probe (Voltage Measurements)

(1) Vds_{driver} (t)

(2) $Vgs_{power\ stage}$ (t)

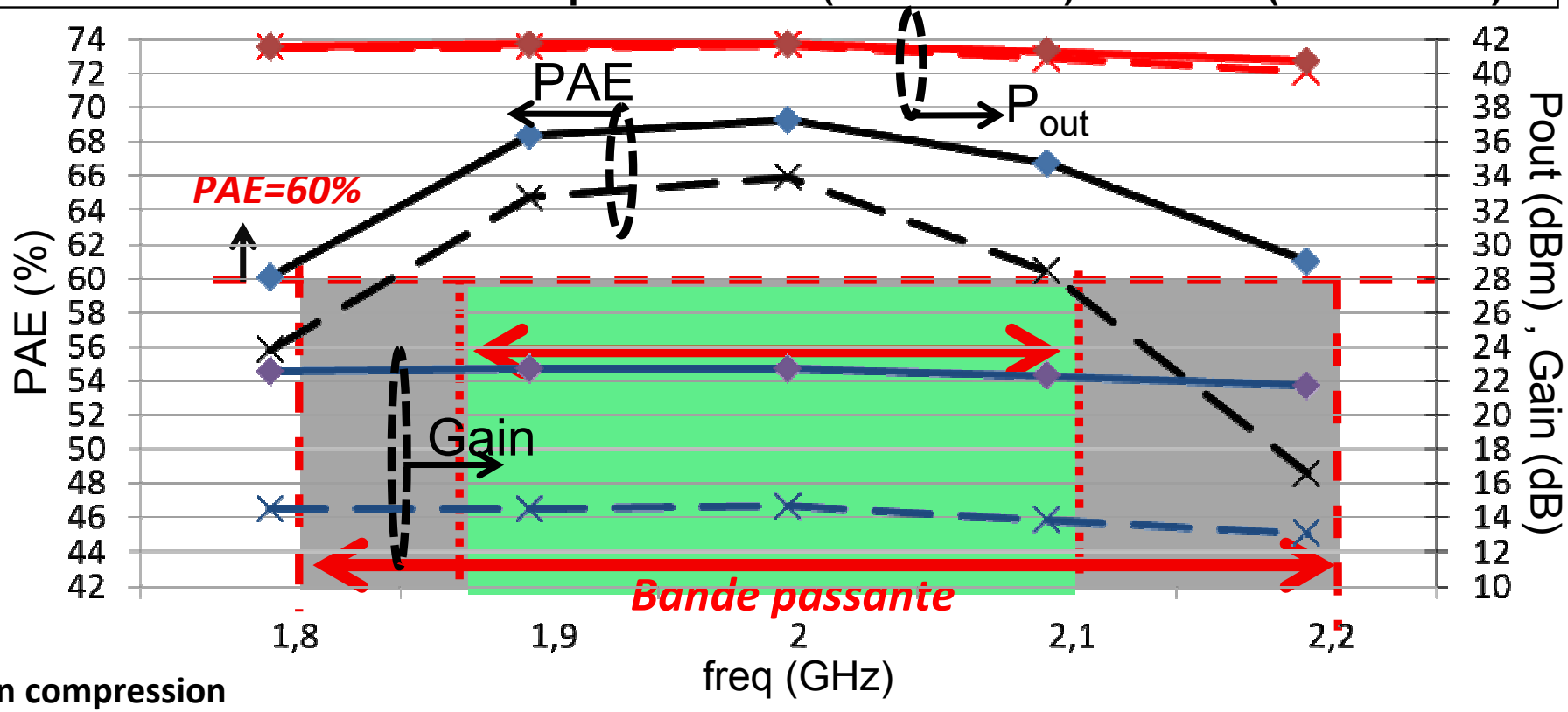
(3) $Vds_{power\ stage}$ (t)





Comparative Measurement Results (RF power and PAE Vs frequency)

Power measurements at connector ports : PA1 (dotted lines) & PA2 (solid lines)

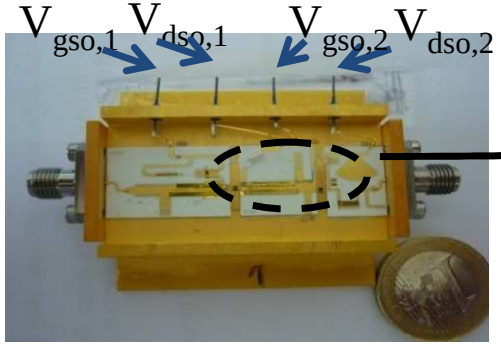


@ about 3dB gain compression

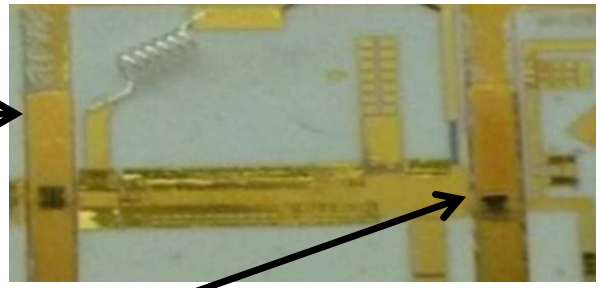
Increase of frequency bandwidth @ PAE> 60%

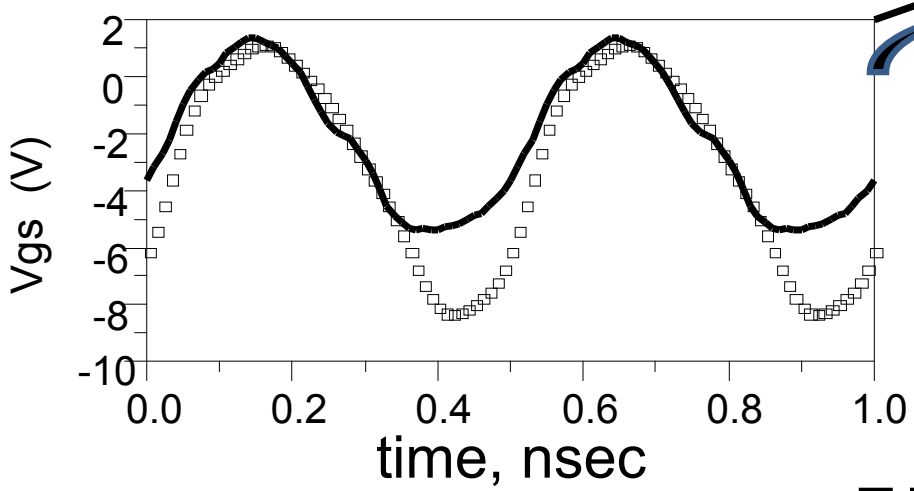
Voltage waveform measurements @ PAE max

Calibrated High impedance probe measurements : Gate source voltage of the power stage of PA2

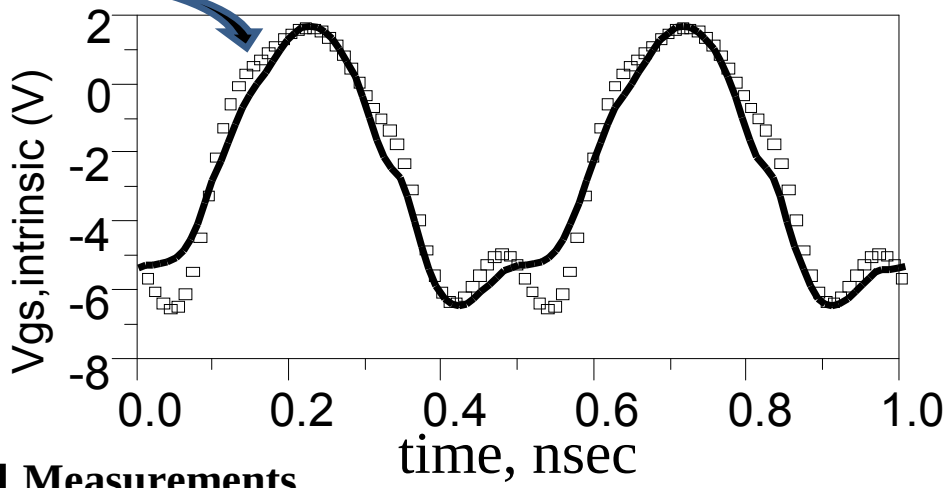


Fo=2Ghz





De-embedded

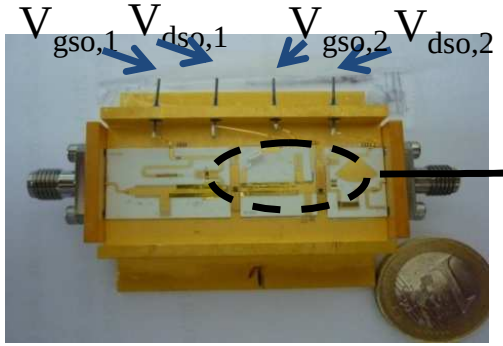


Simulated results

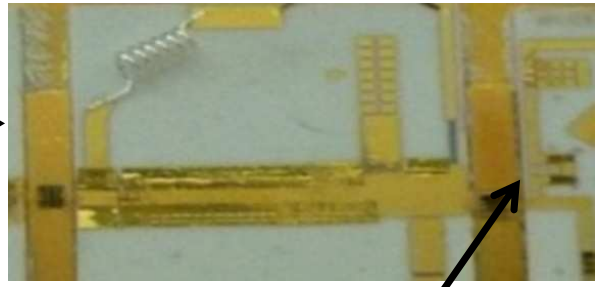
Measurements

Voltage waveform measurements @ PAE max

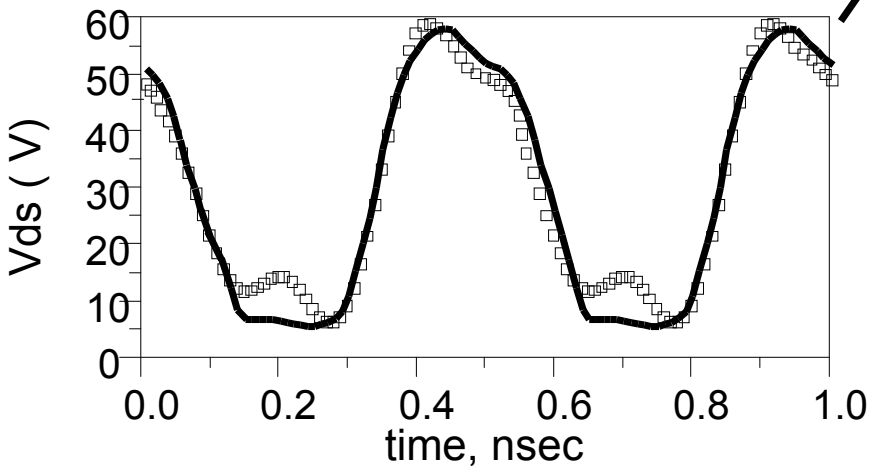
Calibrated High impedance probe measurements : Drain voltage of the power stage of PA2



Fo=2Ghz



Power stage output



Simulated results

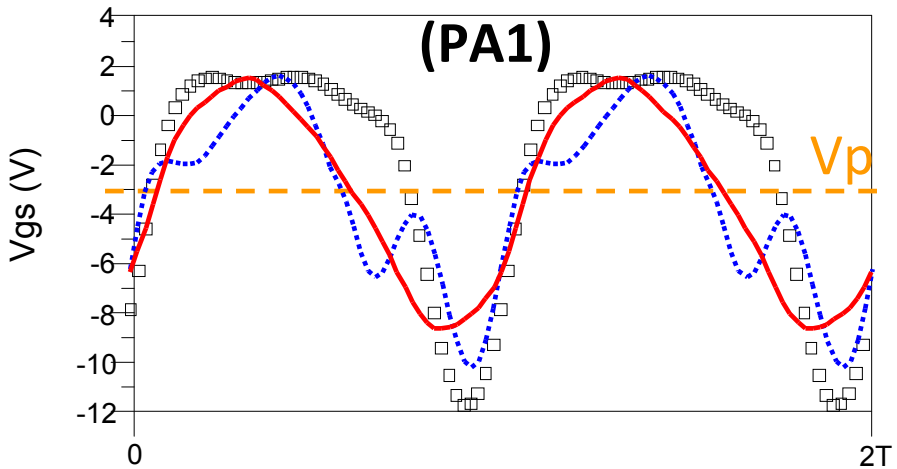
Measurements

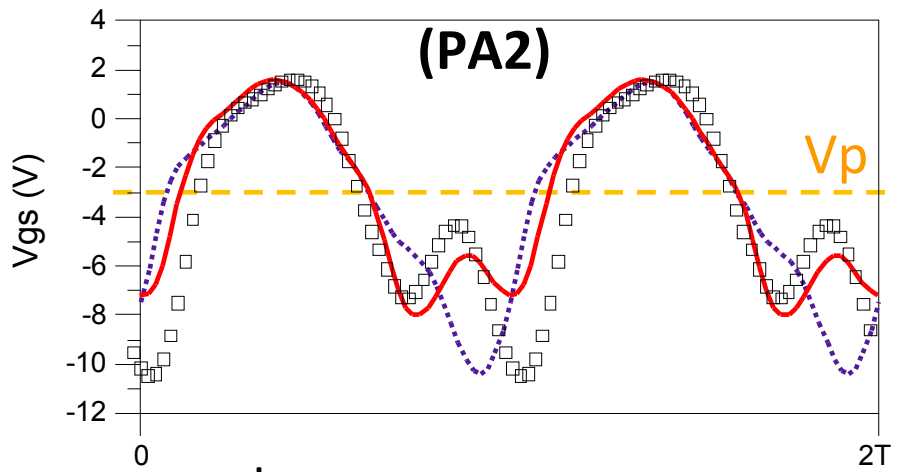
Gate source voltage waveforms (normalized to 2T) measured for different input frequencies

Blue dotted line: 1.8 GHz

Red solid Line : 2 Ghz

Black dotted line: 2.2 Ghz





Gate source voltage of the power stage

For the Two stage power design : Scattering of aperture time is limited when RF frequency is offset each side away center frequency

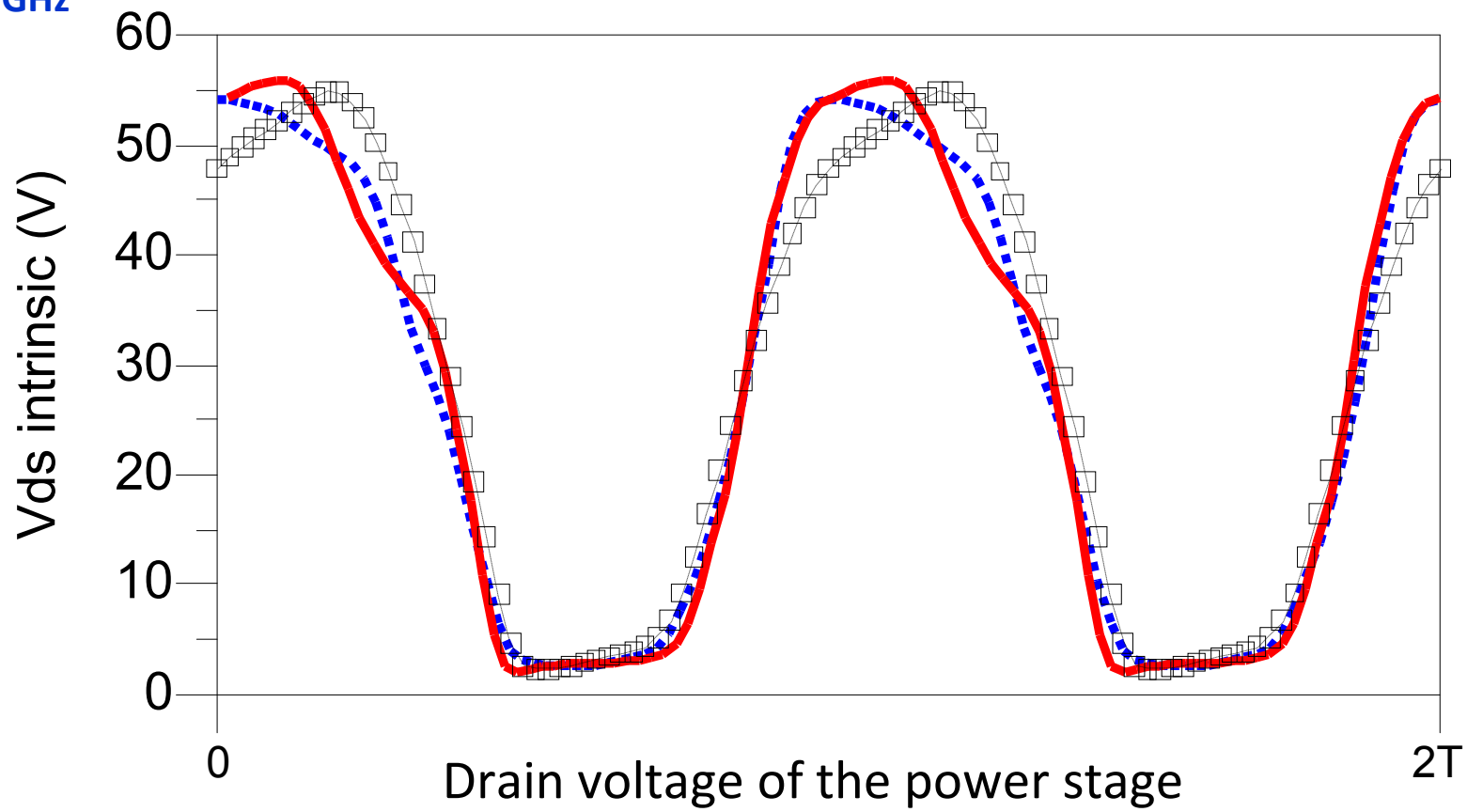
. ➡ **PAE improvement over a wider frequency bandwidth**

Drain voltage waveforms (normalized to 2T) measured for different input frequencies

Blue dotted line: 1.8 GHz

Red solid Line : 2 Ghz

Black dotted line: 2.2 Ghz



iv- Conclusion

To conclude:

- Analysis and design procedures have been carried out using a 'waveform engineering' approach

From preliminar on wafer measurements of a Gan die sample (+ JmT coplanar access) used either for model extraction and load pull measurements

Up to High impedance probing at internal node of a two stage PA (MIC)

Possible future trends

- Characterisation with modulated signals .
- Use of the proposed PA in polar transmitter architectures
- Extension of this work to X Band and MMIC technology